Synchronous-Variable-Frequency Control of Bidirectional DCM Interleaved DC–DC Converter for Wide-Range Enhanced Efficiency

Roberto A. Fantino, *Member, IEEE*, Shamar F. Christian, *Student Member, IEEE*, and Juan C. Balda, *Senior Member, IEEE*

***Abstract*—A bidirectional discontinuous-conduction-mode constant on-time variable-frequency control strategy for a three-phase interleaved dc–dc converter suitable for traction applications is proposed in this article. The strategy enhances the converter efficiency at low-power conditions, providing fairly constant efficiency over the entire power range, by synchronously controlling both the bottom and top switches of the three boost phases. Simulation and experimental results demonstrate the validity and effectiveness of the proposed approach on a 10-kW bidirectional interleaved boost converter.**

***Index Terms*—Bidirectional discontinuous conduction mode (DCM) operation, enhanced efficiency, interleaved boost converters, variable-frequency control.**

I. Introduction

BATTERY-POWERED systems such as electric vehicles (EVs) or energy storages for distributed renewable energy sources are essential in the quest to reduce greenhouse gas emissions on earth [1]. In general, the architecture of these systems is composed of a dc–dc converter for conditioning the voltage level of the battery bank to a higher level required for an inverter stage. This architecture provides advantages regarding the possibility of independent design of the different subsystems, in comparison with systems in which the battery is directly connected to the inverter [2], [3]. Typical EV city driving schedules demand low-power levels from the batteries, most of the time operating at power levels of less than 40% of the nominal rating [4], which makes imperative that the dc–dc converter provides high efficiency at low-power levels to enhance the system performance. Also, bidirectional operation of the dc–dc converter is mandatory for battery power regeneration [5]. The nonisolated half-bridge-based topology (single phase or multiple phase) [6]–[9] is widely used for EVs applications, because of high efficiency, simplicity and reduced number of components in relation with power capability, in comparison with other solutions [4], [5], [10]. Bidirectional dc–dc converters, typically implemented with traditional synchronous complementary continuous-conduction-mode (CCM) pulsewidth-modulation strategies with constant switching frequencies [4]–[6], [11], experience reduced efficiency at low-power levels, because of conduction losses produced by high-frequency currents circulating among the reactive components as well as hard switching losses and diode reverse recovery losses. Alternatively, discontinuous conduction mode (DCM) allows zero-current on-time operation of both bottom and top switching devices, and eliminates diode reverse recovery losses [6]. DCM variable-frequency control techniques allow for the minimization of losses at low-power levels, because the switching frequency and its associated losses are reduced proportionally to the load [12], [13]; no switching is required and no losses are produced in the limit condition of zero load. Variable-frequency control techniques have been widely used in the literature. Among these techniques, constant on-time modulation reports high conversion efficiency under light load conditions [12]–[17]. In [18] and [19], bifrequency high- and low-frequency pulses are used for EMI reduction. Variable-frequency full-range boundary DCM–CCM [20]–[22] and constant off-time control techniques [23] require an increment of the frequency at light load, which increments the frequency associated losses at low power levels. Variable-frequency constant on-time techniques have been usually limited to low-power applications [12]–[15], as switching devices are required to operate with large current peaks that can increase conduction losses. However, in recent years, wide bandgap materials (particularly SiC) are providing MOSFET devices with large current peak capabilities and very low drain-to-source on-resistance, opening the possibility to implement DCM variable-frequency control techniques for high-power applications [24]–[26]. Converters with interleaved operation over the entire power range are usually used to further address the reduction of high-frequency ripple in the current supplied by the battery [6], [8], [27]. However, different studies based on empirical evidence show that no accelerated degradation of batteries occurs at high frequencies, and ripple reduction

Manuscript received January 8, 2021; revised April 24, 2021 and May 29, 2021; accepted June 1, 2021. Date of publication June 24, 2021; date of current version February 1, 2022. This work was supported in part by the University of Arkansas and in part by the National Science Foundation Engineering Research Center for Power Optimization of Electro-Thermal Systems (POETS) under Grant EEC-1449548. *(Corresponding author: Roberto A. Fantino.)*

The authors are with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA (e-mail: rafantin@uark.edu; sc114@uark.edu; jbalda@uark.edu).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TIE.2021.3090718.

Digital Object Identifier 10.1109/TIE.2021.3090718

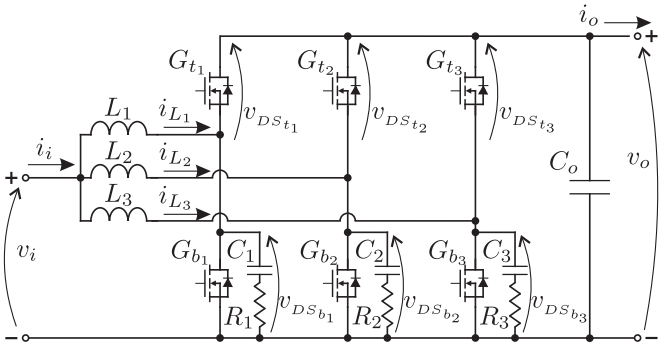


Fig. 1. Bidirectional three-phase interleaved boost dc–dc converter.

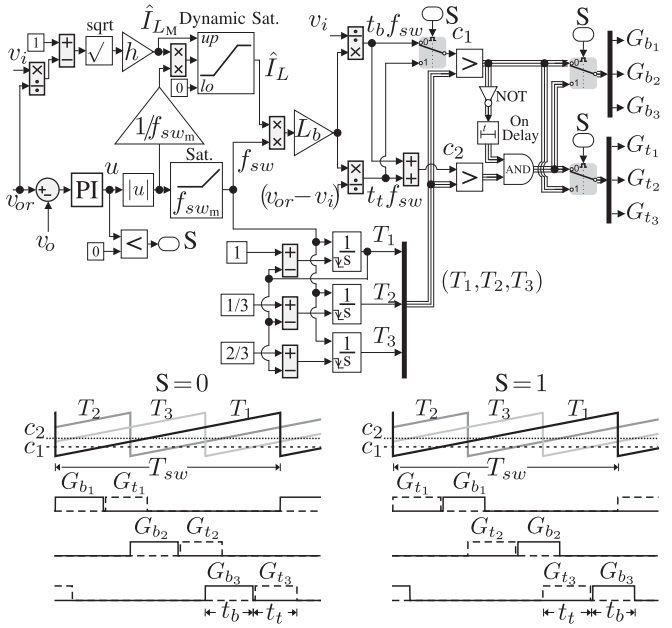


Fig. 2. Block diagram of the control strategy implementation and illustration of the control signals for boost-mode operation ($S = 0$), and buck-mode operation ($S = 1$).

is not needed to be addressed carefully [28], [29], giving the possibility to optimize the converters in terms of cost and efficiency. If necessary, this ripple is normally mitigated by using a capacitor in parallel with the battery bank without compromising efficiency. Additional advantages of DCM operation arises in size reduction of inductors, thus increasing the power density of the overall converter [30], and not having adverse issues associated with inductor current balancing [31].

The goal of this work is to increase the low-power level efficiency of an SiC-based bidirectional three-phase interleaved dc–dc converter suitable for EV applications, through a full DCM variable-frequency control strategy over the full power range. The strategy consists of DCM operation at constant on-time (fixed inductor current peak) while the converter switching frequency is varied according to the operating power requirements. The approach combines the advantages of interleaved operation at medium- and high- power levels, with the advantages of losses reduction by frequency control at low-power levels. Additionally, the proposal provides a mechanism that naturally changes from boost to buck operation allowing bidirectional power flow. Both bottom and top switches of the three phases of the converter are synchronously controlled providing high efficiency over the entire range of operation. A linearized model of the plant suitable for the design of the gains of the controller is provided, together with a complete model of the converter losses that analytically demonstrates that the proposed frequency control allows obtaining fairly constant efficiency through the entire range of operation.

Simulation and experimental results demonstrate the validity and effectiveness of the proposed ideas. A theoretical analysis compared the proposal with three different ones, constant frequency DCM, constant off-time DCM, and boundary DCM–CCM. The experimental validation is implemented on a 10-kW three-phase interleaved boost converter prototype.

II. System Description

This section briefly describes the converter topology and its functionality. Fig. 1 shows the circuit of a bidirectional three-phase interleaved boost dc–dc converter. The dc input voltage v_i from a battery bank, supplies the total input current i_i to the identical inductors $L_1 = L_2 = L_3 = L_B$ (L_B: boost inductance value), corresponding to the three boost phases composed of the bottom switches G_{b_1}, G_{b_2}, and G_{b_3}, and top switches G_{t_1}, G_{t_2}, and G_{t_3}, respectively. The three phases of the converter are connected to the output capacitor C_o that filters the converter output voltage v_o applied to a load represented by the current i_o. The converter operates with $v_o > v_i$ in boost mode (transferring power from the input to the output) and buck mode (transferring power from the output to the input). In boost mode, the bottom switch G_{b_i} $(i = 1, 2, 3)$ is turned ON first during a time t_b in which the inductor L_i is charged, then when G_{b_i} is turned OFF, the inductor discharges its energy to the load during a time t_t in which the top switch G_{t_i} is turned ON for synchronous operation. In buck mode, the switch G_{t_i} is turned ON first during a time t_t in which the inductor is charged, then when G_{t_i} is turned OFF, the inductor discharges its energy to the input during a time t_b in which the bottom switch G_{b_i} is turned ON for synchronous operation. Details of the control algorithm are presented in Section III. The RC snubbers are composed of capacitors $C_1 = C_2 = C_3 = C_s$ (C_s: snubber capacitance value) and resistors $R_1 = R_2 = R_3 = R_s$ (R_s: snubber resistance value), which are needed to damp the DCM inherent resonance produced between the boosting inductors and the parasitic capacitance of the switching devices [32], [33].

III. DCM Control Strategy

This section describes the bidirectional DCM variable-frequency control strategy, and provides a linearized model of the plant suitable to design the gains of the controller. The three boost phases in Fig. 1 are designed to operate under DCM for the entire range of operation. Fig. 2 illustrates the block diagram implementing the proposed variable-frequency DCM control strategy. The three phases operate with switching frequency $f_{\rm sw}$ (switching period $T_{\rm sw} = 1/f_{\rm sw}$), and switching signals delayed

by $T_{\rm sw}/3$ from each other. For given values of v_i and v_o, the converter is controlled by varying $f_{\rm sw}$, whereas the peak value $\hat{I}_L$ of the currents through the inductors (i_{L_1}, i_{L_2}, and i_{L_3}) is kept constant by not changing the on-times of the switches. The error between the measured v_o and the output voltage reference value $v_{\rm or}$ is applied to a proportional–integral (PI) controller. The absolute value $|u|$ of the PI controller output u generates the magnitude of the switching frequency $f_{\rm sw}$. Three equally delayed saw-tooth carriers, T_1, T_2, and T_3, of frequency $f_{\rm sw}$, are generated by using the integrators shown in Fig. 2. In the practical implementation of the converter, these carriers are generated by using the peripheral PWMs of a digital signal processor (DSP). Note that if $v_{\rm or} > v_o$, the signal u is positive and the signal S is zero, corresponding to the condition in which the system delivers power to the output under the boost mode. However, if $v_{\rm or} < v_o$, the signal u is negative and the signal S is 1, which is the alternate condition when the system transfers power from the output to the input under the buck mode. The control signals for both cases $S = 0$ and $S = 1$ are illustrated in Fig. 2. The on-time t_b of the bottom switches and the on-time t_t of the top switches are generated as follows:

$$t_b = L_B \frac{\hat{I}_L}{v_i}, \qquad \text{and} \qquad t_t = L_B \frac{\hat{I}_L}{(v_{\rm or} - v_i)}. \tag{1}$$

Considering an ideal system without losses under steady-state conditions, the output voltage can be represented as

$$v_o = \frac{3}{2} L_B \hat{I}_L^2 \frac{f_{\rm sw}}{i_o} + v_i \tag{2}$$

meaning that for given values of v_i and $\hat{I}_L$, to control the voltage v_o to a specified reference value $v_{\rm or}$, when a load change in i_o occurs, $f_{\rm sw}$ should be modified proportionally to the load change. To ensure DCM through the entire operating range of the converter, L_B must be

$$L_B \le L_{B_{\rm M}} = \frac{3\, V_{i_{\rm m}}^2 (V_{o_{\rm M}} - V_{i_{\rm m}})}{2 V_{o_{\rm M}} P_{o_{\rm M}} f_{{\rm sw}_{\rm M}}} \tag{3}$$

where $P_{o_{\rm M}}$ is the converter maximum output power, $V_{o_{\rm M}}$ is the maximum output voltage, $V_{i_{\rm m}}$ is the minimum input voltage, and $f_{{\rm sw}_{\rm M}}$ is the maximum switching frequency. It is desired to select L_B close to $L_{B_{\rm M}}$ to maximize the overlapping range of the currents of the three inductors. To operate with the same range of frequency variation for full power range, independently of the value of v_i and the desired output voltage $v_{\rm or}$, and with reference to Fig. 2, the inductor current peak is calculated as

$$\hat{I}_{L_{\rm M}} = h \sqrt{1 - \frac{v_i}{v_{\rm or}}} \tag{4}$$

where $h = \sqrt{2P_{o_{\rm M}}/(3 f_{{\rm sw}_{\rm M}} L_B)}$. Note that in Fig. 2, there are two saturation blocks. The block "Sat." limits the minimum operating switching frequency to $f_{{\rm sw}_{\rm m}}$, which is set arbitrarily depending on the application. For example, it can be desired to set $f_{{\rm sw}_{\rm m}}$ beyond the audible noise or beyond the minimum frequency that the digital processor can handle. The block "Dynamic sat." limits the current peak value between zero and the dynamic maximum value $\hat{I}_{L_{\rm M}}$ calculated by (4). Note that when $|u| < f_{{\rm sw}_{\rm m}}$, the system operates at a fixed switching frequency $f_{{\rm sw}_{\rm m}}$ regulating the current peak to a value between $0 \le \hat{I}_L \le \hat{I}_{L_{\rm M}}$. The system is normalized in order to reach $\hat{I}_{L_{\rm M}}$ when $|u| = f_{{\rm sw}_{\rm m}}$. When $|u| > f_{{\rm sw}_{\rm m}}$ the system operates with $\hat{I}_L = \hat{I}_{L_{\rm M}}$, regulating $f_{\rm sw}$.

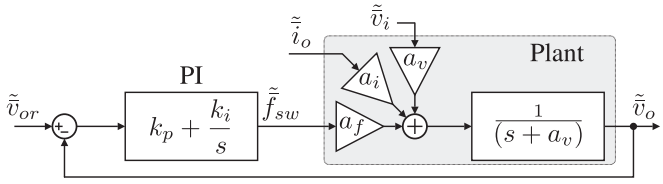


Fig. 3. Linearized plant and control block diagram representation.

A. Plant Model

The gains of the PI controller are determined by modeling the behavior of the output voltage v_o as a function of the control action $f_{\rm sw}$ and any disturbances (e.g., variations of i_o and v_i). The averaged dynamic of v_o can be modeled by [34]

$$\frac{d\bar{v}_o}{dt} = \frac{3\hat{I}_L^2 L_B}{2C_o} \frac{\bar{f}_{\rm sw}}{(\bar{v}_o - \bar{v}_i)} - \frac{\bar{i}_o}{C_o} = \mathbf{g}(\bar{v}_o, \bar{f}_{\rm sw}, \bar{v}_i, \bar{i}_o) \tag{5}$$

where $\bar{v}_o$, $\bar{f}_{\rm sw}$, $\bar{v}_i$, and $\bar{i}_o$ represents the averaged values of the respective variables during a switching interval. To obtain a linear model of the plant at an operating point $A_o = \{\bar{v}_o = V_o, \bar{v}_i = V_i, \bar{f}_{\rm sw} = F_{\rm sw}, \bar{i}_o = I_o\}$, the nonlinear model (5) is linearized using

$$\frac{d\tilde{\bar{v}}_o}{dt} = \left[\frac{\partial \mathbf{g}}{\partial \bar{v}_o}|_{A_o}\right]\tilde{\bar{v}}_o + \left[\frac{\partial \mathbf{g}}{\partial \bar{f}_{\rm sw}}|_{A_o}\right]\tilde{\bar{f}}_{\rm sw} + \left[\frac{\partial \mathbf{g}}{\partial \bar{v}_i}|_{A_o}\right]\tilde{\bar{v}}_i + \left[\frac{\partial \mathbf{g}}{\partial \bar{i}_o}|_{A_o}\right]\tilde{\bar{i}}_o. \tag{6}$$

Applying (6) and the Laplace transformation, the linear model of the plant results

$$\tilde{\bar{V}}_o(s) = \frac{a_f}{(s+a_v)}\tilde{\bar{F}}_{\rm sw}(s) + \frac{a_v}{(s+a_v)}\tilde{\bar{V}}_i(s) + \frac{a_i}{(s+a_v)}\tilde{\bar{I}}_o(s) \tag{7}$$

where $a_f = 3\hat{I}_L^2 L_B/[2C_o(V_o - V_i)]$, $a_v = a_f F_{\rm sw}/(V_o - V_i)$, and $a_i = -1/C_o$. The linearized model of the plant in (7) can be represented by the gray block in Fig. 3. The transfer function of the PI controlled closed-loop system shown in Fig. 3 is

$$\frac{\tilde{\bar{V}}_o(s)}{\tilde{\bar{V}}_{or}(s)} = \frac{a_f k_p (s + k_i/k_p)}{s^2 + (a_v + a_f k_p)s + k_i a_f} \tag{8}$$

where k_p and k_i are the controller proportional and integral gains, respectively. These gains can be designed to obtain a desired behavior of the closed-loop second order system (8), with damping factor $\xi = (a_v + a_f k_p)/(2\sqrt{k_i a_f})$ and natural resonance frequency $\omega_n = \sqrt{k_i a_f}$.

IV. Converter Losses and Efficiency Modeling

In this section, the modeling of the main losses of the converter is presented to demonstrate that the DCM constant on-time variable-frequency control strategy allows us to obtain a fairly constant efficiency over the entire range of operation, highlighting the ability to provide higher efficiency at low-power levels.

A. Inductor Losses

By solving the Improved Generalized Steinmetz Equation [35], the total core losses P_{fe} in the three inductors of the converter can be calculated as

$$P_{fe} = 3V_{fe}k_i\hat{B}^{\beta}\left[t_b^{(1-\alpha)} + t_t^{(1-\alpha)}\right] f_{\text{sw}} = W_{fe}f_{\text{sw}}$$

with

$$k_i = \frac{K_c}{2^{(\beta-1)}\pi^{(\alpha-1)}\left(1.1044 + \frac{6.8244}{\alpha+1.354}\right)}, \tag{9}$$

where α, β, and K_c are the Steinmetz coefficients of the material used for the cores; V_{fe} is the volume of the cores; $\hat{B} = L_B\hat{I}_L/(N_tA_C)$ is the peak flux density within the cores with cross-sectional area A_c, being N_t the number of turns of the windings of the inductors, and $W_{fe} = 3V_{fe}k_i\hat{B}^{\beta}[t_b^{(1-\alpha)} + t_t^{(1-\alpha)}]$.

The rms current circulating through the windings of the inductors can be calculated by $I_{L_{\text{rms}}} = \hat{I}_L\sqrt{(t_b+t_t)f_{\text{sw}}/3}$. By using this value, the copper losses P_{cu} of the three inductors can be represented as

$$P_{\text{cu}} = R_{\text{cu}}\hat{I}_L^2(t_b+t_t)f_{\text{sw}} = W_{\text{cu}}f_{\text{sw}} \tag{10}$$

where R_{cu} is the resistance of the inductors that can be measured at f_{sw_M}, and $W_{\text{cu}} = R_{\text{cu}}\hat{I}_L^2(t_b+t_t)$.

B. Switching Devices Losses

The total conduction losses P_{cd} of both bottom and top switching devices can be calculated as

$$P_{\text{cd}} = R_{\text{on}}\hat{I}_L^2(t_b+t_t)f_{\text{sw}} = W_{\text{cd}}f_{\text{sw}} \tag{11}$$

where R_{on} is the switch on-resistance, and $W_{cd} = R_{\text{on}}\hat{I}_L^2(t_b + t_t)$. The total switching losses can be calculated as follows:

$$P_{\text{sw}} = 3\left(E_{\text{off}} + \frac{1}{2}C_{ds}V_i^2\right)f_{\text{sw}} = W_{\text{sw}}f_{\text{sw}} \tag{12}$$

where E_{off} corresponds to the energy dissipated during the turn-OFF instant of the bottom switch device, a value obtained from the datasheet and a function of $\hat{I}_L$ and V_o. The term $C_{ds}V_i^2/2$ corresponds to the energy of the bottom switch capacitance C_{ds}, which is dissipated when the bottom switch is turned ON. $W_{cd} = 3(E_{off} + \frac{1}{2}C_{ds}V_i^2)$.

The free-wheeling diode losses of the top switch can be approximated as

$$P_{fd} = 3V_{fd}\hat{I}_Lt_Df_{\text{sw}} = W_{fd}f_{\text{sw}} \tag{13}$$

where t_D is the turn-ON dead-time of the top switch, V_{fd} is the forward-bias voltage of the free-whiling diodes of the devices, and $W_{fd} = 3V_{fd}\hat{I}_Lt_Df_{\text{sw}}$.

C. Gate Charge Losses

These losses are related to the charge and discharge of the gate input capacitance of the MOSFETs (C_{iss} in data-sheets) during the switching process [36]. It can be estimated as

$$P_{gc} = 6C_{\text{iss}}\Delta V_{\text{GS}}^2f_{\text{sw}} = W_{gc}f_{\text{sw}} \tag{14}$$

where ΔV_{GS} is the variation of the gate-to-source voltage of the MOSFETs between the turn-ON and the turn-OFF transitions, and $W_{gc} = 6C_{\text{iss}}\Delta V_{\text{GS}}^2$. In typical applications, these losses are negligible compared with the main loss mechanisms of the converter.

By combining (11)–(13), the total losses in the switching devices can be represented as

$$P_M = P_{cd} + P_{\text{sw}} + P_{fd} + P_{gc} = W_Mf_{\text{sw}} \tag{15}$$

where $W_M = W_{cd} + W_{\text{sw}} + W_{fd}$.

D. Snubber Losses

The total losses in the snubbers can be approximated as [32]

$$P_{sn} = 3C_{sn}V_o^2f_{\text{sw}} = W_{sn}f_{\text{sw}} \tag{16}$$

where $W_{sn} = 3C_{sn}V_o^2$.

E. Output Capacitor Losses

The total rms current circulating through the output capacitor can be approximated by the combined effect of the currents of the three top switches of the converter. This is a conservative approximation because the capacitor rms current at high power is reduced due to overlapping and output dc current. With this consideration, the losses P_{C_o} in C_o, can be approximated by

$$P_{C_o} \approx R_{C_o}\hat{I}_L^2t_tf_{\text{sw}} = W_{C_o}f_{\text{sw}} \tag{17}$$

where R_{C_o} is the equivalent series resistance of the output capacitor, and $W_{C_o} = R_{C_o}\hat{I}_L^2t_t$.

F. Total Losses and Efficiency

The mean value of the converter input power can be expressed as

$$P_i = \frac{3}{2}V_i\hat{I}_L(t_b+t_t)f_{\text{sw}} = W_{P_i}f_{\text{sw}} \tag{18}$$

where it is defined $W_{P_i} = \frac{3}{2}V_i\hat{I}_L(t_b+t_t)$. By using (9)–(18), the efficiency of the converter can be expressed as

$$\eta = 1 - \frac{W_{fe} + W_{cu} + W_M + W_{sn} + W_{C_o}}{W_{P_i}}. \tag{19}$$

For given values of the input and output voltages, W_{fe}, W_{cu} W_M, W_{sn}, W_{C_o}, and W_{P_i} are constants independent of the switching frequency and load current, meaning that the addressed DCM constant on-time variable-frequency control method provides constant efficiency (19) over the entire power range.

V. Simulation Results

Simulation results of the control strategy described in Section III are presented in this section. Also, theoretical losses analysis by using the losses modeling described in Section IV is performed. The losses, efficiency, and input current ripple of the proposed constant turn-ON variable-frequency DCM control are compared with three different control strategies, constant frequency DCM, constant off-time DCM, and boundary DCM–CCM. In order to simulate the proposed strategy in a realistic

TABLE I
SIMULATION AND EXPERIMENTAL SYSTEM PARAMETERS

Symbol	Value	Symbol	Value
$V_{o_m} - V_{o_M}$	600 V – 800 V	P_{o_n}; P_{o_M}	10 kW; 12 kW
$V_{i_m} - V_{i_M}$	250 V – 400 V	$f_{sw_m} - f_{sw_M}$	2 kHz – 50 kHz
L_B	100 μH	K_c	0.2281
α; β	1.5319; 1.9532	V_{fe}	110 cm^3
A_c	3.12 cm^2	N_t	15 Turns
C_s; R_s	0.33 nF; 900 Ω	R_{on}; V_{fd}	43 mΩ; 3.3V
E_{off}	0.3 mJ [a]	C_{ds}; C_{iss}	220 pF; 2.8 nF
C_o; ΔV_{GS}	120 μF; 25 V	k_p; k_i	36; 2160

[a] @ $V_{ds} = 800$ V; $I_d = 50$ A

scenario, the most important characteristics of a bidirectional three-phase interleaved boost dc–dc converter prototype were simulated in MATLAB/SIMULINK. The converter, of nominal power P_{o_n}, nominal input voltage $V_{i_n} = 300$ V and nominal output voltage $V_{o_n} = 600$ V was implemented with turn-ON dead-time $t_D = 0.5$ μs. All the parameters used to implement the simulation are listed in Table I, and are the same of the experimental prototype addressed in Section VI. By replacing the corresponding parameters in (3), it results $L_{B_M} = 107.4$ μH and $L_B = 100$ μH is used for the implementation. The gains k_p and k_i of the controller have been calculated to obtain damping factor $\xi = 1/\sqrt{2}$, and a 5% settling time $t_{s_{5\%}} = 0.05$ s that can be approximated doing $\omega_n = 3/(t_s\xi)$ [37], considering the worst case scenario for the damping factor of (8), that occurs when $a_v = 0$.

Fig. 4(a) shows the converter losses calculated by using (9)–(17) with the parameters in Table I, for the case in which the converter in Fig. 1 is controlled applying the proposed constant on-time variable-frequency control strategy for $v_i = V_{i_n}$ and $v_o = V_{o_n}$. It can be seen that the variation of all the losses is proportional to the converter power. Fig. 4(b) shows the same losses for the case in which the converter is operated under DCM but with a fixed frequency $f_{sw} = f_{sw_M}$ and the output voltage is controlled by varying the on-time of the switches. Fig. 4(c) shows the same losses for the DCM constant off-time case, and Fig. 4(d) for the boundary DCM-CCM case. Fig. 4(e) displays the converter efficiency and Fig. 4(f) the rms value $I_{i_{rms}}$ of the converter input current i_i for the four cases. Table II lists the equations of f_{sw} and $\hat{I}_L$ used to calculate the losses (9)–(17) as a function of P_o, and the values of f_{sw}, $\eta\%$, $I_{i_{rms}}$, P_M, P_{cd}, and P_{sw} evaluated for $P_o = P_{on}/10$ and $P_o = P_{on}$.

Note that in Table II, the full range boundary DCM–CCM condition requires a 10× increase of f_{sw} from $P_o = P_{on}$ to $P_o = P_{on}/10$, resulting in a drastic reduction of the converter efficiency under light load conditions due to the increase of the frequency associated losses. As can be seen in Fig. 4(d) and Table II, the constant on-time case provides a considerably greater efficiency at low-power levels compared with the other control cases. In fact, the efficiency for the DCM frequency control case remains fairly constant [according to (19)], until the switching frequency reaches its minimum value f_{sw_m} and

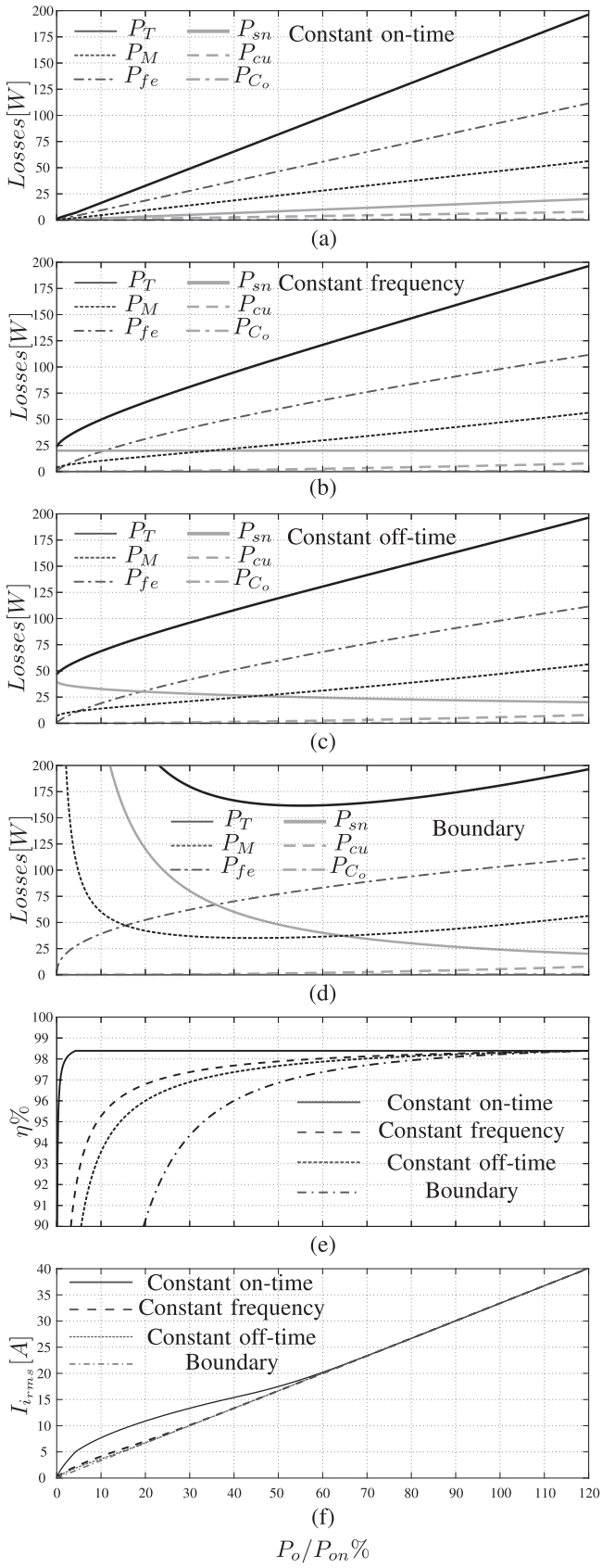


Fig. 4. Theoretical analysis for $v_i = V_{i_n}$ and $v_o = V_{o_n}$. (a) Constant on-time DCM losses. (b) Constant frequency DCM losses. (c) Constant off-time DCM losses. (d) Boundary DCM-CCM losses. (e) Efficiency comparison. (f) $I_{i_{rms}}$ comparison.

TABLE II
COMPARISON BETWEEN FOUR DCM CONTROL STRATEGIES (DATA EVALUATED FOR $v_i = V_{i\mathrm{N}}$ AND $v_o = V_{o\mathrm{N}}$)

Parameter	Constant on-time DCM	Constant frequency DCM	Constant off-time DCM	Boundary DCM-CCM
f_{sw}	$\frac{2(v_o - v_i)L_B}{3v_i^2 t_b^2} i_o$ $t_b = \frac{2L_B P_{oM}}{3v_i^2}$	$\frac{3v_i^2(v_o - v_i)L_B}{2P_{oM}L_B v_o}$	$\frac{1}{t_{off}} + \frac{\lambda i_o - \sqrt{4t_{off}\lambda i_o + \lambda^2 i_o^2}}{2t_{off}^2}$ $\lambda = \frac{(v_o - v_i)L_B}{3v_i^2}$; $t_{off} = \frac{2L_B P_{oM}}{3v_i^2}$	$\frac{3v_i^2(v_o - v_i)}{2L_B v_o^2} \frac{1}{i_o}$
$\hat{I}_L$	$\frac{2P_{oM}}{3v_i}$	$\sqrt{\frac{2(v_o - v_i)i_o}{3L_B f_{sw}}}$	$\frac{v_i}{L_B}\left(\frac{1}{f_{sw}} - t_{off}\right)$	$\frac{2v_o i_o}{3v_i}$
f_{sw} @ $P_o = P_{on}/10$	4.16 kHz	50 kHz	82 kHz	600 kHz
f_{sw} @ $P_o = P_{on}$	41.6 kHz	50 kHz	53 kHz	60 kHz
η% @ $P_o = P_{on}/10$	98.5%	95.6%	94.1%	76.5%
η% @ $P_o = P_{on}$	98.5%	98.4%	98.4%	98.3%
$I_{i_{rms}}$ @ $P_o = P_{on}/10$	7.6 A	4.2 A	3.7 A	3.35 A
$I_{i_{rms}}$ @ $P_o = P_{on}$	33.5 A	33.5 A	33.5 A	33.5 A
P_M @ $P_o = P_{on}/10$	4.5 W	10 W	13.7 W	62.3 W
P_M @ $P_o = P_{on}$	45.2 W	45.2 W	45.3 W	45.6 W
P_{cd} @ $P_o = P_{on}/10$	2.54 W	0.74 W	0.58 W	0.21 W
P_{cd} @ $P_o = P_{on}$	25.4 W	23.3 W	22.6 W	21.2 W
P_{sw} @ $P_o = P_{on}/10$	1.74 W	8.16 W	11.48 W	53.64 W
P_{sw} @ $P_o = P_{on}$	17.4 W	19.4 W	20.06 W	21.56 W

duty cycle control is implemented at very low-power levels. As can be seen in Table II, the constant on-time case has the highest conduction losses P_{cd} at low power levels, due to higher rms current in the switching devices. However, this is overcompensated by a larger reduction of P_{sw} in comparison with the other control strategies (for which the switching losses are dominant at low-power levels), resulting in the lowest total losses in the switching devices for the constant turn-on strategy. The cost of the high efficiency provided by the constant on-time variable-frequency strategy, is a higher $I_{i_{\mathrm{rms}}}$ at low-power levels with respect to the other strategies. This is because of the input current ripple due to a nonoverlapping of the currents through the inductors at low-frequency operation. However, as the power increases, the input current ripple is reduced due to overlapping and the value of $I_{i_{\mathrm{rms}}}$ tends to the mean value of i_i, which is the same as the other control techniques. If it is required for the application (as can be the case of a high series resistance battery), the input current ripple at low-power levels can be mitigated without compromising the efficiency placing a low ESR capacitor in parallel with the voltage source [9].

The waveforms in Fig. 5 correspond to the simulation results for the cases in which the converter operates at $P_o = P_{\mathrm{on}}/10$ and $P_o = P_{\mathrm{on}}$. Fig. 5(a_1) shows the gate signals G_{b_1} and G_{t_1} of one of the boost phases for $P_o = P_{\mathrm{on}}/10$. Fig. 5(b_1) shows the gate-to-source voltages of the bottom switch $v_{gs_{b_1}}$ and top switch $v_{gs_{t_1}}$ of one of the boost phases for $P_o = P_{\mathrm{on}}/10$. Fig. 5(c_1) shows the converter input current i_i and the currents through the inductors i_{L_1}, i_{L_2} and i_{L_3}, for $P_o = P_{\mathrm{on}}/10$. The same corresponding waveforms are shown in Fig. 5(a_2)–(c_2) for the case $P_o = P_{\mathrm{on}}$. In Fig. 5(c_1) it can be seen that at low-power, nonoverlapping is observed and the magnitude of the ripple in i_i is the same as the currents through the inductors (with three times the frequency). Furthermore, Fig. 5(c_2) verifies the reduction in the input current ripple produced by the overlapping of the currents through the inductors at high-power levels.

Figs. 6 and 7 present simulation results evaluating the ability of the bidirectional constant on-time variable-frequency control strategy (see Fig. 2) to regulate the converter output voltage to $V_{\mathrm{or}} = 600$ V for $v_i = 300$ V. For the simulation in Fig. 6, a resistor of 45 Ω is initially connected to the output of the converter. At the instant $t = 0.25$ s the load is abruptly changed to 65 Ω, at the instant $t = 1$ s the load is changed back to 45 Ω, and at the instant $t = 1.25$ s an increase of 20 V in the reference V_{or} is implemented. Fig. 6(a) compares the response in the voltage v_o for the simulation of the system in Fig. 1 with the simulation results of the linearized model in Fig. 3. Even when the perturbations applied to the system are not small signal variations, the behavior of the linearized model closely matches with the simulation results of the real system. Fig. 6(b) displays the current i_i, Fig. 6(c) the current i_{L_1}, and Fig. 6(d) the switching frequency f_{sw}. The inductor current peak value $\hat{I}_L$ remains constant while the frequency is changed by the controller to regulate v_o.

A load current i_o of 1.857 A is initially applied to the output of the converter to test its bidirectional operation and control strategy. With reference to Fig. 6, the current load is changed to -1.857 A at $t = 0.5$ s (changing the direction of the power flow), and at $t = 1.25$ s the current is returned to its initial value. For this test, Fig. 6(a)–(d) illustrates the same waveforms in Fig. 5. In Fig. 6(a), a large overvoltage is observed in v_o after the direction of the converter output current changed; then, the controller immediately reverses the direction of the currents through the inductors to modify the direction of the power flow and regulate v_o. In Fig. 6(d), during transitions, the switching

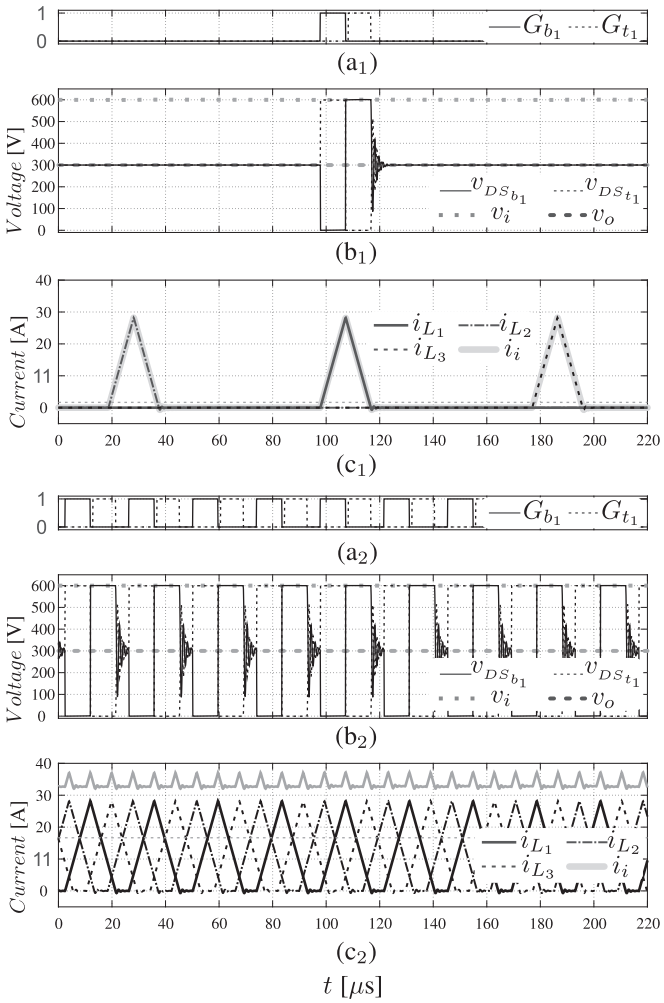


Fig. 5. Simulation results for $P_o = P_{\text{on}}/10$, $f_{\text{sw}} = 4.16$ kHz. (a$_1$) G_{b_1} and G_{t_1}; (b$_1$) $v_{\text{GS}_{b_1}}$ and $v_{\text{GS}_{t_1}}$; (c$_1$) i_i, i_{L_1}, i_{L_2}, and i_{L_3}. Simulation results for $P_o = P_{\text{on}}$, $f_{\text{sw}} = 41.6$ kHz: (a$_2$) G_{b_1} and G_{t_1}; (b$_2$) $v_{GS_{b_1}}$ and $v_{GS_{t_1}}$; (c$_2$) i_i, i_{L_1}, i_{L_2}, and i_{L_3}.

frequency f_{sw} reaches its minimum value f_{sw_m} limited by the block "Sat." shown in Fig. 2.

VI. Experimental Results

In this section, experimental results of the control strategy described in Section III are presented, using a 10-kW interleaved boost converter. A photo of the experimental setup used for the implementation is shown in Fig. 8. The controller is implemented by using a DSP TMS320F28379D. The converter prototype is built using C2M0025120D SiC MOSFET devices, along with IXD609 MOSFET drivers with 5-Ω gate resistors, powered by +20/-5 V isolated power supplies MGJ2D122005SC. The inductors are built using nanocrystalline cores KMNC-50 and Litz wire with 315 strands of diameter 0.12 mm. Three 40 μF B32778 G TDK capacitors make up the output capacitance. Table I contains all the parameters of the experimental system, which are the same ones used in the simulations presented in Section V. Similar tests to those presented in Section V are

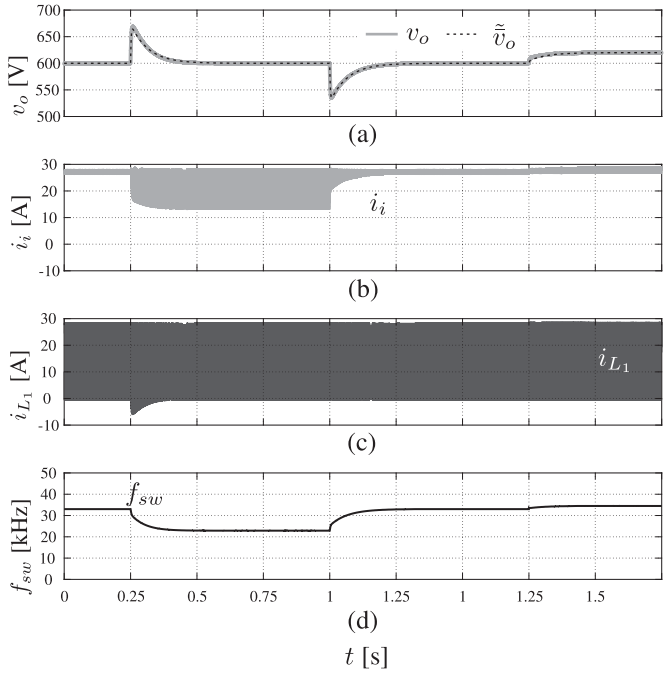


Fig. 6. Simulation results. (a) v_o. (b) i_i. (c) i_{L_1}. (d) f_{sw}. Load change from 45 Ω to 65 Ω at $t = 0.25$ s. Load change from 65 Ω to 45 Ω at $t = 1$ s. Step in V_{or} from 600 V to 620 V at $t = 1.25$ s.

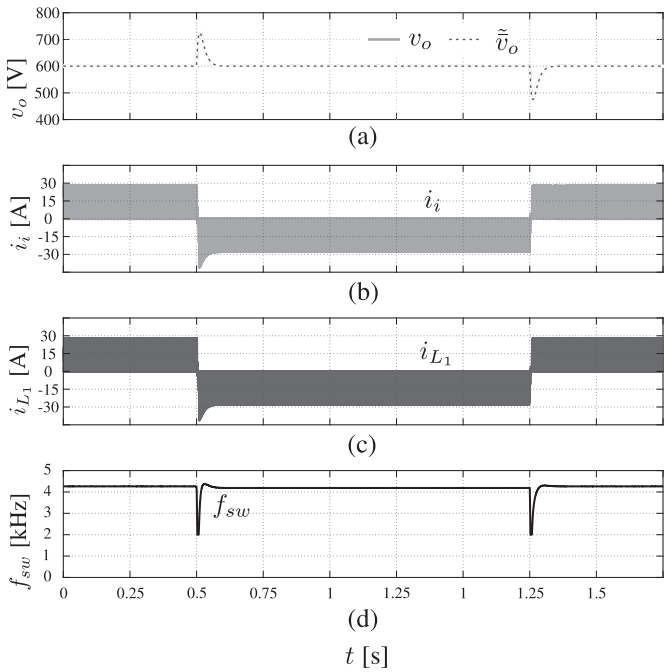


Fig. 7. Simulation results. (a) v_o. (b) i_i. (c) i_{L_1}. (d) f_{sw}. Test of bidirectional operation. Step in i_o from 1.857 A to −1.857 A at $t = 0.5$ s, and from −1.857 A to −1.857 A at $t = 1.25$ s.

implemented in order to corroborate experimentally the control strategy.

In Fig. 9, the experimental waveforms $v_{GS_{b_1}}$, $v_{GS_{t_1}}$, $v_{DS_{b_1}}$, $v_{DS_{t_1}}$, v_i, v_o, i_i and i_{L_1}, are similar the simulation results shown in Fig. 5. The waveforms in Fig. 9(a) correspond to the case in which the converter operates at $P_o = P_{\text{on}}/10$ with

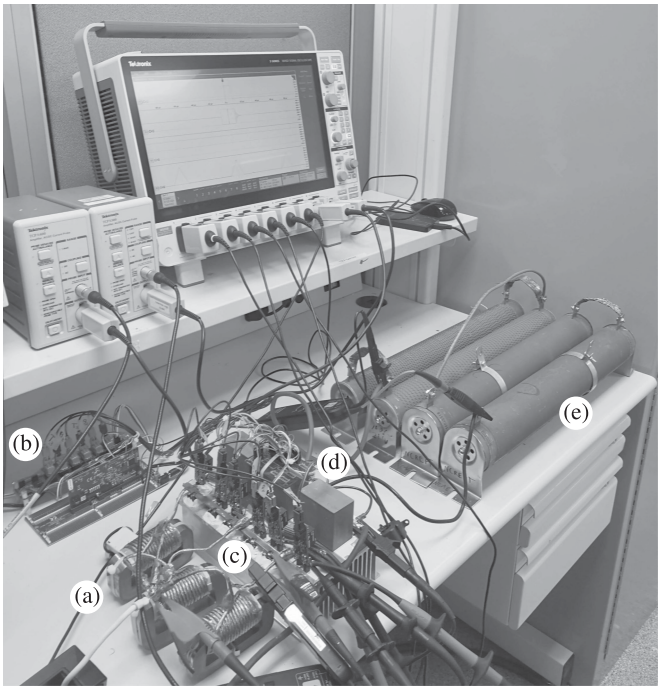


Fig. 8. Experimental setup. (a) Inductors. (b) DSP. (c) Heat-sink mounted MOSFETs. (d) Capacitors. (e) Load resistors.

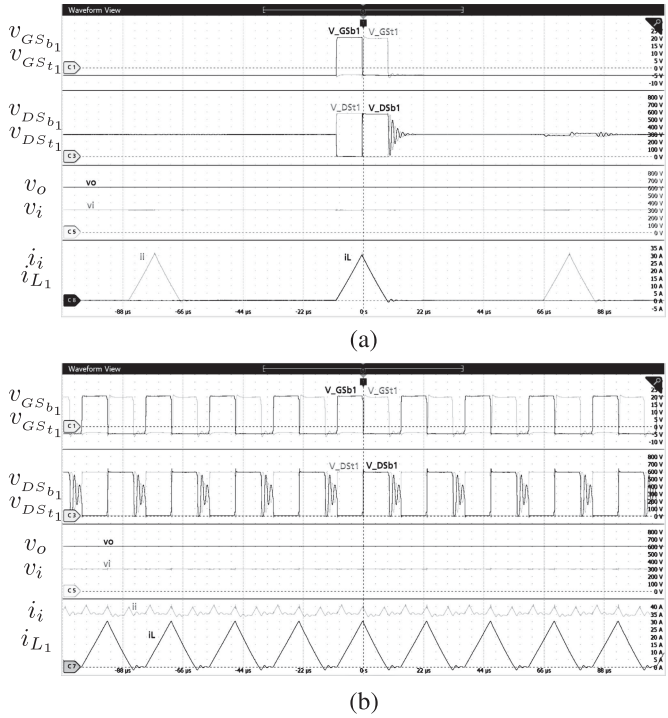


Fig. 9. Experimental results. (a) $v_{GS_{b_1}}$, $v_{GS_{t_1}}$, $v_{DS_{b_1}}$, $v_{DS_{t_1}}$, v_i, v_o, i_i and i_{L_1} for $P_o = P_{\text{on}}/10$, $f_{\text{sw}} = 4.16$ kHz. (b) $v_{GS_{b_1}}$, $v_{GS_{t_1}}$, $v_{DS_{b_1}}$, $v_{DS_{t_1}}$, v_i, v_o, i_i and i_{L_1} for $P_o = P_{\text{on}}$, $f_{\text{sw}} = 41.6$ kHz. Time scale: 22 μs/div; Vertical scales: 5 V/div, 100 V/div, 100 V/div, 5 A/div.

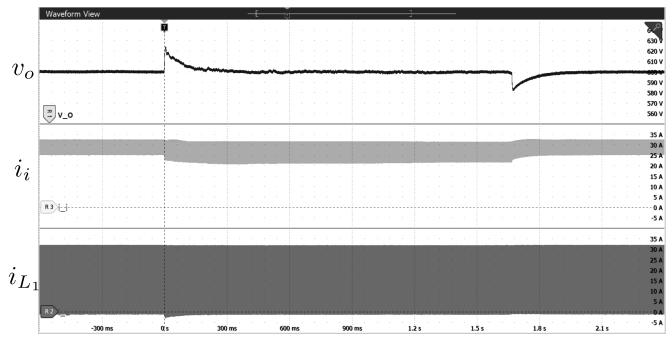


Fig. 10. Experimental results. v_o, i_i and i_{L_1} for a load change from 45 Ω to 65 Ω and from 65 Ω to 45 Ω. Time scale: 300 ms/div; Vertical scales: 10 V/div, 5 A/div, 5 A/div.

$f_{\text{sw}} = 4.16$ kHz, and the waveforms in Fig. 9(b) to the case in which the converter operates at $P_o = P_{\text{on}}$ with $f_{\text{sw}} = 41.6$ kHz. These results verify the reduction in the ripple present in i_i at high-power levels; however, the ripple is not uniform because of slight differences between the values of the three inductors.

Fig. 10 shows the experimental waveforms v_o, i_i, and i_{L_1} when the load changes from 45 to 65 Ω and then back to 45 Ω. This test was implemented by connecting a 45- Ω resistor in series with a 20- Ω resistor, the last one with a parallel switch that gives the possibility of adding or removing it. The variation in the output voltage is less than the variation observed in Fig. 6 for the same simulation test. This difference can be due to the parasitic components of the resistors and the switch, which makes the resistance variation an imperfect step. However, v_o is regulated to $V_{\text{or}} = 600$ V after each perturbation with the same dynamics shown in the simulation results, corroborating experimentally the validity of the model used to design the gains of the controller.

The experimental setup used to test the bidirectional operation of the converter is illustrated in Fig. 11(a). Two unidirectional dc voltage sources are used, one operating at 300 V and another at 650 V. The diodes D_1 and D_2 are used to protect the sources from negative current flows. Initially the switch "sw" is open and the 300- V input source is supplying 1.8 kW to the 50- Ω resistor and 1.028 kW to the 350- Ω resistor connected to the output of the converter that regulates v_o to $V_{\text{or}} = 600$ V. When "sw" is closed, the 650 V source delivers 2.166 kW through the 15 Ω resistor, supplying 1.028 kW to the 350 Ω and the remaining power to the 50 Ω at the input of the converter. A capacitor $C_a = 1.2$ mF was used at the input to absorb the negative current ripple and keep v_i constant as in a battery application. Fig. 11(b) shows the experimental waveforms v_o, i_i, and i_{L_1} for the instants in which "sw" is closed and opened again. After "sw" closes, the input voltage first increases to 650 V but it is then regulated by the boost converter to $V_{\text{or}} = 600$ V operating now with negative current flow. When "sw" is opened, a similar response to the one in Fig. 7 is observed. The results shown in Fig. 11(b) corroborate experimentally the ability of the proposed DCM control strategy to regulate the output voltage for bidirectional power flow operation.

Fig. 12 shows the experimental efficiency measured for the variable-frequency constant on-time control case and the comparison with the constant frequency case. In particular, a considerable amount of points were taken for $P_o/P_{\text{on}} < 30\%$, corroborating experimentally that the DCM constant on-time

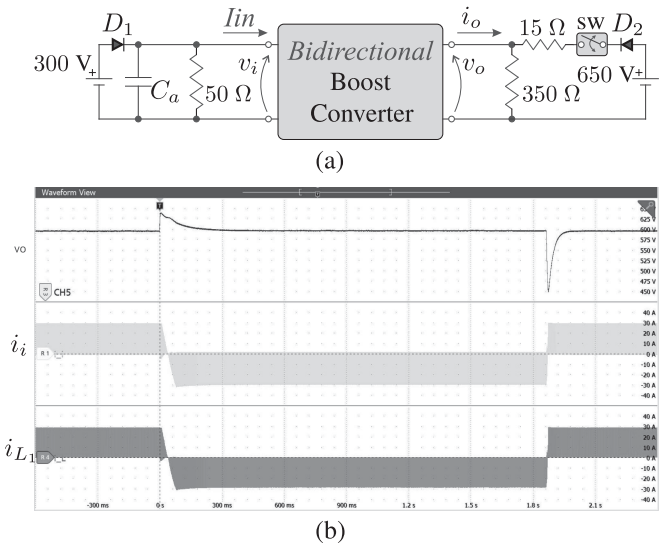


Fig. 11. Experimental results. (a) Experimental setup used to implement the bidirectional power flow test. (b) v_o, i_i and i_{L_1} for a change in i_o from 1.7 A to -1.63 A and from -1.63 A to 1.7 A. Time scale: 300 ms/div; Vertical scales: 25 V/div, 10 A/div, 10 A/div.

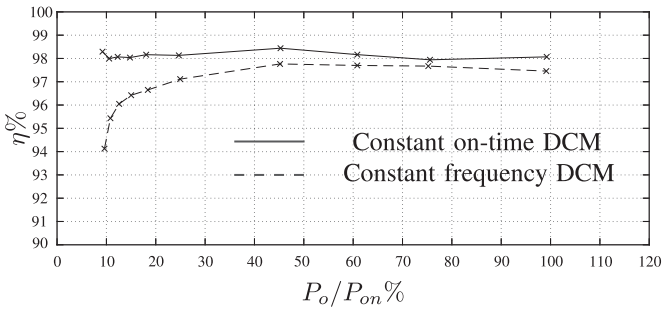


Fig. 12. Experimental efficiency. Comparison between variable-frequency constant on-time DCM and constant frequency DCM.

variable-frequency control strategy provides a considerable improvement in the efficiency at low-power levels, and a practically constant efficiency $\eta\% >= 98\%$ over the entire range of variable-frequency operation. It is worth mentioning that general purpose inductors were used for the implementation, even greater values of efficiency can be obtained through the design optimization of the inductors.

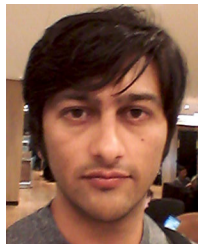
VII. Conclusion

A full power range DCM constant on-time variable-frequency control strategy for a bidirectional three-phase interleaved dc–dc converter suitable for EVs applications was presented in this article. A theoretical comparison against three different control strategies (fixed-frequency, constant off-time, and boundary DCM–CCM condition) demonstrated that the proposal provides a significant increment of the converter efficiency at low-power levels, and provided fairly constant efficiency over the entire range of operation. The penalty for higher efficiency was a higher rms input current at low-power levels in comparison with the other strategies, caused by the ripple due to the nonoverlapping of the currents through the inductors at low-frequency operation. When required by the application (as can be the case of a battery with a high series resistance), the input current ripple at low-power levels can be mitigated without compromising the efficiency by placing a low equivalent series resistance (ESR) capacitor in parallel with the voltage source. The performance of the controller was successfully evaluated through dynamic and bidirectional operation experimental tests. A fairly constant efficiency $\eta\% \geqslant 98\%$ was experimentally measured over the entire range of the converter operation.

References

[1] A. Y. Saber and G. K. Venayagamoorthy, "Plug-in vehicles and renewable energy sources for cost and emission reductions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1229–1238, Apr. 2011.
[2] J. Lai and D. J. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicles," *Proc. IEEE*, vol. 95, no. 4, pp. 766–777, 2007.
[3] C. C. Chan, "The state of the art of electric, hybrid, and fuel cell vehicles," *Proc. IEEE*, vol. 95, no. 4, pp. 704–718, Apr. 2007.
[4] H. Chen, H. Kim, R. Erickson, and D. Maksimović, "Electrified automotive powertrain architecture using composite dc-dc converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 98–116, Jan. 2017.
[5] S. Dusmez, A. Hasanzadeh, and A. Khaligh, "Comparative analysis of bidirectional three-level DC-DC converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3305–3315, May 2015.
[6] D. Kim, G. Choe, and B. Lee, "DCM analysis and inductance design method of interleaved boost converters," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4700–4711, Oct. 2013.
[7] M. W. Beraki, J. P. F. Trovão, M. S. Perdigão, and M. R. Dubois, "Variable inductor based bidirectional DC-DC converter for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 66, no. 10, pp. 8764–8772, Oct. 2017.
[8] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 578–586, May 2006.
[9] J. M. Blanes, R. Gutiérrez, A. Garrigós, J. L. Lizán, and J. M. Cuadrado, "Electric vehicle battery life extension using ultracapacitors and an FPGA controlled interleaved buck-boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5940–5948, Dec. 2013.
[10] R. Schupbach and J. Balda, "Comparing DC-DC converters for power management in hybrid electric vehicles," in *Proc. IEEE Int. Elect. Mach. Drives Conf.*, vol. 3, 2003, pp. 1369–1374.
[11] A. Vazquez, A. Rodriguez, M. R. Rogina, and D. G. Lamar, "Different modular techniques applied in a synchronous boost converter with SiC MOSFETs to obtain high efficiency at light load and low current ripple," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8373–8382, Oct. 2017.
[12] C. Qiao and J. Zhang, "Control of boost type converter at discontinuous conduction mode by controlling the product of inductor voltage-second," in *Proc. IEEE 36th Power Electron. Specialists Conf.*, 2005, pp. 1213–1219.
[13] R. Erickson and D. Maksimović, "High efficiency DC-DC converters for battery-operated systems with energy management," Dept. Elect. Comput. Eng., Univ. Colorado, Boulder, CO, USA, 1999.
[14] B. Sahu and G. A. Rincon-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time pulse-frequency modulation (PFM) control," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 54, no. 2, pp. 312–321, Feb. 2007.
[15] B. Arbetter and D. Maksimovic, "Control method for low-voltage dc power supply in battery-powered systems with power management," in *Proc. 28th Annu. IEEE Power Electron. Specialists Conf. Formerly Power Conditioning Specialists Conf. 1970-71. Power Process. Electron. Specialists Conf.*, vol. 2, 1997, pp. 1198–1204.
[16] J. Wang, J. Xu, and B. Bao, "Analysis of pulse bursting phenomenon in constant-on-time-controlled buck converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5406–5410, Dec. 2011.
[17] N. Kong, D. S. Ha, J. Li, and F. C. Lee, "Off-time prediction in digital constant on-time modulation for DC-DC converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2008, pp. 3270–3273.
[18] J. Wang and J. Xu, "Peak current mode bifrequency control technique for switching dc-dc converters in DCM with fast transient response and low EMI," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1876–1884, Apr. 2012.

[19] J. Xu and J. Wang, "Bifrequency pulse-train control technique for switching DC-DC converters operating in DCM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3658–3667, Aug. 2011.
[20] T. Song and H. S. Chung, "Boundary control of boost converters using state-energy plane," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 551–563, Mar. 2008.
[21] M. Biglarbegian, N. Kim, and B. Parkhideh, "Boundary conduction mode control of a boost converter with active switch current-mirroring sensing," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 32–36, Jan. 2018.
[22] T. Konjedic, L. Koročec, M. Truntič, C. Restrepo, M. Rodič, and M. Milanovič, "DCM-based zero-voltage switching control of a bidirectional DC-DC converter with variable switching frequency," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3273–3288, Apr. 2016.
[23] K. Hariharan, S. Kapat, and S. Mukhopadhyay, "Constant off-time digital current-mode controlled boost converters with enhanced stability boundary," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10270–10281, Oct. 2019.
[24] M. Imaizumi *et al.*, "Remarkable advances in SiC power device technology for ultra high power systems," in *Proc. IEEE Int. Electron Devices Meeting*, 2013, pp. *6.5.1–6.5.4.*
[25] A. Merkert, J. Müller, and A. Mertens, "Component design and implementation of a 60 kW full SiC traction inverter with boost converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.
[26] Z. Ni, Y. Li, C. Liu, M. Wei, and D. Cao, "A comparison of 100 kW SiC DC-DC converters for electric vehicles," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2019, pp. 1–6.
[27] D. Joo, D.-H. Kim, and B.-K. Lee, "DCM frequency control algorithm for multi-phase DC-DC boost converters for input current ripple reduction," *J. Elect. Eng. Technol.*, vol. 10, pp. 2307–2314, Nov. 2015.
[28] M. J. Brand, M. H. Hofmann, S. S. Schuster, P. Keil, and A. Jossen, "The influence of current ripples on the lifetime of lithium-ion batteries," *IEEE Trans. Veh. Technol.*, vol. 67, no. 11, pp. 10 438–10445, Nov. 2018.
[29] P. Ferraz and J. Kowal, "A comparative study on the influence of DC/DC-converter induced high frequency current ripple on lithium-ion batteries," *Sustainability*, vol. 11, Oct. 2019, Art. no. 6050.
[30] J. Zhang, J. Lai, R. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc-dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.
[31] H. Chen, C. Lu, and U. S. Rout, "Decoupled master-slave current balancing control for three-phase interleaved boost converters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3683–3687, May 2018.
[32] R. Lan and N. Rossetti, "Correct snubber power loss estimate saves the day," *HOW2POWER TODAY*, Dec. 2016. [Online]. Available: http://www.how2power.com/pdf_view.php?url=/newsletters/1612/articles/H2PToday1612_design_Maxim.pdf
[33] M. Walczak, "Impact of inductor current ringing in DCM on output voltage of DC-DC buck power converters," *Arch. Elect. Eng.*, vol. 66, pp. 313–323, Jun. 2017.
[34] S. Chiniforoosh *et al.*, "Definitions and applications of dynamic average models for analysis of power systems," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2655–2669, Oct. 2010.
[35] W. Hurley and W. Wölfle, *Transformers and Inductors for Power Electronics: Theory, Design and Applications (Ingenieria Electrica)*. Hoboken, NJ, USA: Wiley, 2013.
[36] *Application Note: Calculation of Power Loss (Synchronous)*, *Rohm Semiconductor*, Kyoto, Japan, 2016.10-Rev. 003, Oct. 2016.
[37] K. Ogata, *Modern Control Engineering (Instrumentation and Controls Series)*. London, U.K.: Pearson, 2010. [Online]. Available: https://books.google.com/books?id=Y49iPwAACAAJ

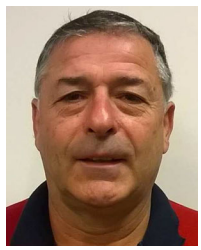


Roberto A. Fantino (Member, IEEE) received the B.Sc. degree in electronics engineering, the M.S. degree in electrical engineering, and the Ph.D. degree in control systems from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 2011, 2015, and 2018, respectively.

From 2012 to 2019, he was with the Departamento de Ingeniería Eléctrica y de Computadoras, Instituto de Investigaciones en Ingeniería Eléctrica Alfredo C. Desages, Universidad Nacional del Sur, where he was a Graduate Teaching Assistant. He is currently a Postdoctoral Research Fellow with the University of Arkansas, Fayetteville, AR, USA. His research interests include power electronics, grid power control, renewable and alternative energy resource, automotive applications, and distributed power generation.

Shamar F. Christian (Student Member, IEEE) received the B.Sc. degree in electrical engineering from Howard University, Washington, DC, USA. He is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA.

His current research interests include power electronic converters, automotive applications, and high-frequency and high-power magnetic design.



Juan C. Balda (Senior Member, IEEE) received the B.Sc. degree from the Universidad Nacional del Sur, Bahía Blanca, Argentina, in 1979, and the Ph.D. degree from the University of Natal, Durban, South Africa, in 1986, both in electrical engineering.

He was first employed as a Researcher and a part-time Lecturer with the University of Natal until July 1987. He spent two years as a Visiting Assistant Professor with Clemson University, Clemson, SC, USA. Since July 1989, he has been with the University of Arkansas, Fayetteville, AR, USA, where he is currently a University Professor, Department Head, Associate Director for applications of the National Center for Reliable Electric Power Transmission (NCREPT). His main research interests include power electronics, electric power distribution systems, motor drives, and electric power quality.

Dr. Balda is a member of the Power Electronics and Power & Energy Societies, and the honor societies Eta Kappa Nu and Tau Beta Pi. He is also the Chair of IEEE PELS TC5 Committee and Faculty Advisor to the local chapter of the IEEE Power Electronics Society.