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A Medium-Voltage SiC Flying Capacitor Converter Design for 25-kV Distribution Systems

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***Abstract*— Grid-connected medium-voltage (MV) distribution flexible ac transmission systems (D-FACTS) can be used to perform many functions such as improving the quality of electric power in distribution systems. This paper provides a design methodology for a 2-MVA MV D-FACTS based on a flying-capacitor converter (FCC) topology for three-phase four-wire 25-kV distribution systems. By considering the breakdown and utilization voltages of the available power modules as the main design factor, 10-kV silicon-carbide (SiC) MOSFET half-bridge power modules was chosen with 73% utilization factor. Then, sizing of the flying capacitor cells, dc-bus capacitance, and output LCL filter was performed. Thereafter, the required parts for these components were selected to show the feasibility of fabrication. The power losses of switching modules were investigated for one phase of the converter. Finally, the envisioned MV-FCC functions of compensating for three-phase unbalanced currents and injecting reactive power complementing switched capacitor banks are illustrated through simulations.**

Keywords*— *Multilevel converter, Unbalanced Current Static Compensator, 10-kV SiC MOSFET, D-FACT

I. INTRODUCTION

In general, distribution systems are used to supply different types of loads which are divided into two main categories; three-phase loads and single-phase ones. The latter type is mainly composed of residential loads that change according to consumer's consumption and lead to unbalanced loading of distribution systems. Load imbalances have the potential of getting worse due to the proliferation of single-phase rooftop solar systems. The imbalance problem worsens distribution voltage profile as well as feeder negative- and zero-sequence current components [1-6]. Several issues are produced by these current components such as reduced system efficiency, neutral conductor overloading, transformers overheating, and generated magnetomotive force (MMF) ripples in grid-connected electric machines [7, 8].

Shunt-connected compensators can be used to eliminate these current components and their effects so upstream equipment may have a balanced load. These converters are called medium-voltage distribution flexible ac transmission systems (MV D-FACTS) and can perform other functions like reactive power compensation, harmonic currents mitigation, enhancing the distribution voltage levels, and reducing the system power losses [9-12]. There are several MV D-FACTS topologies but multilevel converters have more advantages such as eliminating coupling step-up transformers by connecting directly the D-FACTS to the distribution system, however, the number of power devices as well as the complexity of the converter system are increased [13].

Multilevel converters produce a multi-step voltage waveform with controllable and variable amplitude, frequency, and phase by connecting power semiconductors and capacitive voltage sources properly. The number of levels of a synthesized voltage waveform depends on the number of constant voltage values or steps that can be produced between the output terminal and internal reference called neutral. The four main multilevel converter topologies are cascade H-bridge converter (CHBC), diode-clamped converter (DCC), flying capacitor converter (FCC), and modular multilevel converter (MMC) [13-16].

For reactive power compensation and current compensation specifically, the CHB is not suitable for a neutral-point-clamped (NPC) configuration as it cannot be easily configured to share energy between the phases. The main disadvantage of DCC is that the number of diodes increases exponentially with the number of required levels and the conduction losses can increase drastically as a result. The MMC is convenient due to its fully modular nature but suffers from requiring large capacitances (that are inversely proportional to the line frequency). The FCC suffers from an exponential increase in the number of flying capacitors as the levels increase, but the amount of the required capacitance is inversely proportional to the switching frequency (not the line frequency as in the MMC case) and the effective switching frequency is the switching frequency of a switching position times the number of levels minus one [17].

By using silicon carbide (SiC) MOSFETs, the switching frequency can be significantly increased when compared to Si IGBTs, and thus significantly decrease both size and cost of the flying capacitor (FC), and reduce filter requirements [14, 18]. Consequently, the FCC topology was chosen for designing a 25-kV, 2-MVA unbalanced current static compensator (MV-UCSC) based on SiC MOSFET half-bridge power modules; its main specifications are given in Table I. The main functions of this MV-UCSC are compensating for negative- and zero-sequence currents as well as reactive power currents complementing conventional capacitor banks. In general, optimum design of this FCC-based MV-UCSC is a challenging task which based on many factors like the number of voltage levels, switching and conduction losses, total harmonic distortion, and system complexity.

The objectives of this paper are then designing the proposed MV-UCSC, evaluating converter efficiency, sizing the various

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components and selecting their parts. So, the remaining of this paper is organized as follows: the design methodology of MV-UCSC power stage is presented in section II, selection of the components is shown in section III, different MV-UCSC losses such as module, dc-link, FC, and output filter losses are analyzed and calculated in section IV, simulation results of the selected design are evaluated in section V, and conclusions and future work are given in section VI.

II. Design Methodology of the 25-kV 2-MVA UCSC Power Stage

The neutral-point-clamped (NPC)-based FCC topology has series-connected capacitors with two switching positions as clamped switching cells. The voltages of both the FC cells and dc-link capacitors are combined to form the ac output voltage levels. The number of these levels depends on various parameters like switching frequency, THD of the ac voltage waveform, and system costs [14, 18]. However, the breakdown voltage of the selected devices is considered as the main design factor. So, the design methodology starts by selecting the appropriate power module, and then sizing the other components of the converter power stage (i.e., FC cells, dc-link capacitors, and the output filter).

A. SiC MOSFET Half-Bridge Power Modules

Due to the superior advantages of SiC MOSFET, different engineering samples of half-bridge power modules have been characterized and investigated by both power semiconductor companies and researchers. These samples have rated voltage of 3.3-kV, 6.5-kV, 10-kV, and 15-kV with different current capabilities [18-21]. Initial comparison between these modules, which is illustrated in Table II, showed that 10-kV SiC MOSFET half-bridge power modules offer good compromise between system complexity and converter losses. These modules have ideal operating voltage range from 7.2 kV to 7.6 kV and their switching frequency can be up to 10 kHz [22].

Thus, a three-phase seven-level MV-UCSC design is proposed with one phase shown in Fig. 1. Switching positions S1 to S12 require 6 half-bridge modules per phase. By controlling these switching positions, a seven-level output voltage V_{ph} can be synthesized and can be calculated as follows:

$$V_{ph} = -\frac{V_{dc}}{2} + S_6\, x\, V_{dc} + \sum_{i=1}^{i=5}\left[(S_i - S_{i+1})\, x\, \frac{i}{6}\, V_{dc}\right] \quad (1)$$

where V_{dc} is the total dc-link voltage, S_1 to S_6 represent the state of each switching position (1 if closed and 0 if opened). Each phase has five FC cells; $C_1 - C_5$, where C_1 is composed of one FC unit, C_2 two FC units and so on. Under steady-state conditions, the rated voltage of C_1, C_2, C_3, C_4, and C_5 should be (1⁄6) V_{dc}, (2⁄6) V_{dc}, (3⁄6) V_{dc}, (4⁄6) V_{dc}, and (5⁄6) V_{dc}, respectively.

B. Flying and DC-link Capacitors

After selecting the suitable power module, the minimum required capacitance of each FC unit C_{fc} can be calculated using the following equation [23]:

$$C_{fc} \geq \frac{1}{\Delta V_{fc}} \hat{I}_s \frac{1}{2\, f_{sw}} (1 - m_a) \quad (2)$$

where ΔV_{fc} is the desired ripple voltage across one unit, $I_{s,pk}$ is the peak of the sinusoidal current, f_{sw} is the switching frequency of a submodule, and m_a is the modulation index.

The minimum dc-link capacitance C_{dc} is given by [16]:

$$C_{dc} \geq \frac{\hat{I}_s}{\Delta V_{dc}\, \omega_g} \quad (3)$$

where ΔV_{dc} dc is the desired voltage ripple of the dc bus, and ω_g is the grid angular frequency. The required capacitances of C_{dc} and C_{fc} are shown Tables I & II, respectively.

C. Output LCL Filter

The LCL filter topology chosen to fulfill IEEE 519 requirements offers a better decoupling between filter and grid impedances. The parameters of LCL filter were calculated based on the analysis presented in [24-26] as follows:

1) The filter capacitance

The filter capacitance C_f depending on the converter power rating is chosen as a percentage of the base capacitance. This percentage should be less than 2% to minimize the consumed reactive power. So, C_f is calculated as follows:

$$C_f \leq \frac{0.02\, S_{conv}}{V_{LL,rms}{}^2\, \omega_g} \quad (4)$$

So, C_f is 170 nF at only 2% of the converter power.

2) The converter-side inductor

The converter-side inductor L_c is mainly used for smoothing the ripples of switching frequency current and is inversely proportional to the switching frequency. It is determined using:

Table I. MAIN SPECIFICATIONS OF THE PROPOSED MV-UCSC.

Parameter	Value
Rated voltage $V_{LL,rms}$	25 kV
Rated power S_{conv}	2 MVA
Rated current $I_{conv,rms}$	46.2 A
Grid frequency f_g	60 Hz
Switching frequency f_{sw}	10 kHz
DC-link voltage V_{dc}	44 kV
DC-link Capacitance C_{dc} at 5% voltage ripple	160 µF

Table II. COMPARING DESIGN PARAMETERS OF MV-UCSC USING DIFFERENT SIC MOSFET POWER MODULES

Parameter	**3.3-kV-based MV-FCC**	**6.5-kV-based MV-FCC**	**10-kV-based MV-FCC**	**15-kV-based MV-FCC**
No. of levels	19	11	7	5
No. of power modules	18 x 3	10 x 3	6 x 3	4 x 3
Utilization voltage	2.44 kV (74%)	4.4 kV (67%)	7.33 kV (73%)	11 kV (73%)
Level flying capacitance	3 µF	2 µF	1 µF	0.5 µF
No. of FC Cells	17 x 3	9 x 3	5 x 3	3 x 3

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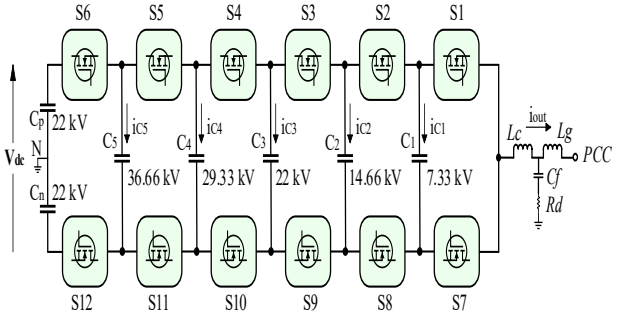

Fig. 1. 7-level MV-UCSC using 10-kV SiC MOSFET half-bridge power modules.

$$L_c = \frac{V_{C1}}{\Delta i_c \, I_L \, f_{eff}} \tag{5}$$

where V_{C1} is the voltage of first level of the MV-UCSC, Δi_c the chosen output current ripple percentage, I_L the load current rating, and f_{eff} the effective output frequency of the MV-UCSC. The target converter-side inductance equals 3.8 mH.

3) The grid-side inductor

The grid-side inductor L_g also mitigates current harmonics. So, it is chosen to satisfy the following conditions:

$$\Delta i_g = \frac{1}{\left|1+r\left(1-L_c C_f \left(2\pi f_{eff}\right)^2\right)\right|} \tag{6}$$

$$L_g = r \, L_c \tag{7}$$

where r is the ratio between L_g and L_c and Δi_g is the percent current ripple reduction of the grid-side inductor. Both inductors should reduce the ripple of the output current to 5% or less. The required grid-side inductance for the MV-UCSC is then calculated iteratively in a Matlab™ script and solving for r. For simplicity of construction and lower THD at initially lower test currents, the L_g was made identical to L_c ($r = 1$).

4) The damping resistance

The last part of the output filter is the damping resistance which is used to reduce possible resonances and prevent system instability. The required damping resistance R_f can be determined as follows:

$$R_f = \frac{1}{3 \, \omega_{res} C_f} \tag{8}$$

$$\omega_{res} = \sqrt{\frac{L_c + L_g}{L_c L_g C_f}} \tag{9}$$

where ω_{res} is the angular resonant frequency for the LCL filter. The required damping resistance for the MV-FCC is 23 Ω.

III. Selecting the Suitable Components for the Proposed MV-UCSC

Based on the minimum requirements, dc-link, FC unit, and filter capacitors were selected from available off-the-shelf parts, while the filter inductors were custom designed.

A. Dc-Link Capacitors

Choosing the dc-link capacitor type was mostly dependent on the energy density. Besides, a large capacitance is needed for the standard NPC type converter. So, electrolytic capacitors met these requirements since they have advantages in terms of great energy density and significant current capability at large values of capacitance. Also, load currents flow into these capacitors, so, their equivalent series inductance (ESL) is not considerable. However, they are not as reliable and have higher parasitics compared to other capacitor types.

Based on available parts, each dc-bus capacitor (i.e., C_p and C_n) consists of 52 electrolytic capacitors, which their rated values are 11,000 µF and 550 V, in series to achieve a sufficient overvoltage margin of 28 kV. In Fig. 2, a model of one of the dc-bus capacitors is shown where the 52 capacitors are divided into two groups for easier installation and structure stability.

B. FC Capacitors

For the FC capacitance, film capacitor type was selected. In spite of having lower energy density than electrolytic capacitors, and having higher parasitic ESL than ceramic technologies, film capacitors have better reliability than other types. Metallized film capacitors have two features; one is self-healing after high current transients, while the other one is failing in an open state. The last feature is important since it is required that no FC units fail short because of the semi-modular characteristic of the FC multi-level inverter.

The ESL of the FC stacks is an important aspect for many reasons including EMI, voltage spikes across the devices, voltage balancing, and output voltage distortion. One way to reduce the ESL is paralleling several strings of capacitors. Moreover, paralleling multiple smaller rating capacitors provides more control over the form factor of the capacitor stacks. By selecting a suitable part, the FC unit will consist of 8 capacitors rated 12µF and 1200 V, in series to form a string, with 4 strings connected in parallel. Due to the high voltage of FC stacks (e.g., $V_{C2} = 14.66\ kV$), an isolation material was used to meet both clearance and creepage standards [27]. A model of C_2 stack is shown in Fig. 3 which consists of two C_{fc} units connected in series and between them an isolation material.

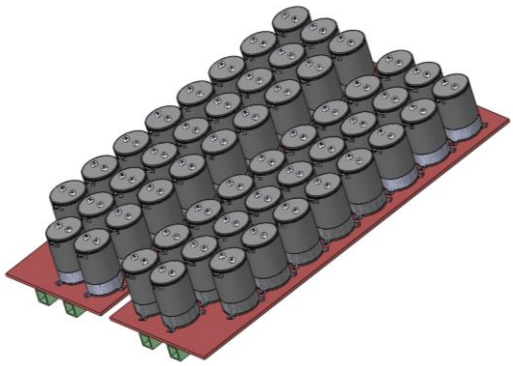

Fig. 2. Model of the dc-bus capacitance

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C. Filter Capacitor

Film capacitor technology was also chosen for filter capacitor. This type has a non-negligible equivalent series resistance (ESR) so that the actual damping resistor will be less than the required 23 Ω. By selecting SCRN film capacitor type with rated values of 3μF and 2 kV_{pk}, 14 units will be connected in series. A model of the filter capacitors is presented in Fig. 4.

D. Filter Inductors

Both filter inductors (L_c and L_g) were designed based on [26]. Hitachi MetGlas® Amophous C-Cores (AMCC-1000 equivalent) were selected as the cores of the inductors, while custom wires were designed to form the windings. A model is displayed in Fig. 5.

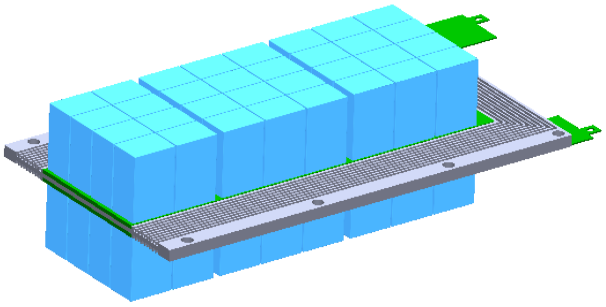

Fig. 3. FC-C2 model.

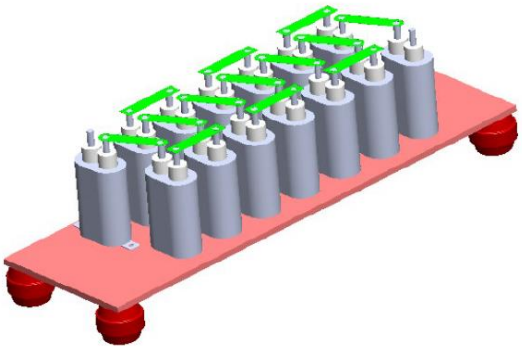

Fig. 4. Model of the filter capacitance.

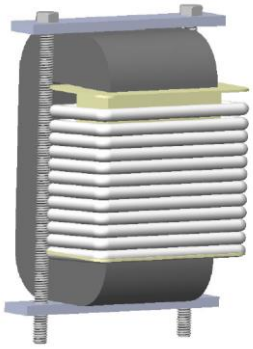

Fig. 5. Model of the filter inductor.

IV. Analytical Evaluation of the 10-kV-Based 7-Level MV-UCSC

The proposed MV-UCSC is evaluated by calculating power losses of the converter power stage. These losses can be divided into two main categories; conduction and switching. All passive components encounter only conductions losses while the power modules have both of them. By using analytical equations, power losses can be determined which depend on number of switching-power-cell and voltage levels, load PF, converter output power, and modulation index.

Moreover, phase-shift pulse width modulation (PS-PWM) is utilized. Consequently, required stepped output voltage are generated, natural voltage balancing of FCs is guaranteed, and all converter cells operate with identical periods because the charging and discharging intervals of two different switching states have the same duty cycle [28].

A. Power Loss Calculations of 10-kv SiC MOSFET Half-Bridge Power Modules

The average value of conduction losses per one converter phase P_{cond} can be calculated by:

$$P_{cond} = N * \left[R_{DSon}.{I_{Drms}}^2 + u_{D0}.I_{Fav} + R_D.{I_{Frms}}^2\right] \quad (10)$$

where N equals the number of output voltage levels minus one, R_{DSon} is the drain-source on-state resistance, I_{Drms} the SiC MOSFET rms on-state current, u_{D0} the diode on-state zero-current voltage, I_{Fav} the average diode current, R_D the diode on-state resistance, and I_{Frms} the rms diode current. It should be noted that N modules are conducting over one PWM cycle.

The average value of switching losses per one converter phase P_{sw} can be determined as follows:

$$P_{sw} = 2N * f_{sw} * \left(E_{onM} + E_{offM} + E_{onD}\right) \quad (11)$$

where E_{onM} is the SiC MOSFET turn-on energy losses, E_{offM} is the SiC MOSFET turn-off energy losses, and E_{onD} is the diode reverse-recovery energy. While all required parameters depend on the characteristics of the power module, the required currents can be calculated as follows [28]:

$$I_{Drms} = I_p \sqrt{(1/8) + (m_a/3\pi)\, x\, cos(\varphi_L)} \quad (12)$$

$$I_{Fav} = I_p\, .\, ((1/2\pi) - (m_a/8)\, x \cos(\varphi_L)) \quad (13)$$

$$I_{Frms} = I_p \sqrt{(1/8) - (m_a/3\pi)\, x\, cos(\varphi_L)} \quad (14)$$

where I_p is the peak current, and φ_L is the load phase angle between phase voltage and current. So, the power losses of modules can be determined per one phase of the converter separately according to the operating condition since each phase has different ones in case of MV-UCSC application.

B. FC Cell and DC-bus Capacitor Losses

The type of capacitor element would affect its losses. For example, the ESR of electrolytic capacitors varies with frequency while it is approximately constant in film capacitors.

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The capacitor losses can be determined according to the analysis in [29] as follows:

$$E_{cap} = \int_{t0}^{t} C^2 \left(\frac{\mathrm{dV}}{\mathrm{dt}}\right)^2 . (ESR)\, dt \quad (15)$$

$$P_{avg_{cap}} = f_{sw} . E_{cap} \quad (16)$$

where E_{cap} is the capacitor energy loss, C is the capacitance.

C. Output LCL Filter Losses

Both, fundamental- and high-frequency currents generate power losses in the filter which can be divided into two parts: damping losses and inductors losses. Inductors losses include copper, iron, and airgap losses [25, 26].

V. Simulation Results of the Proposed 25-kV 2-MVA MV-UCSC

The grid-connected MV-UCSC was simulated using Matlab/Simulink™. In Fig. 6, both converter and grid line-to-neutral voltage are compared to give context to the converter output waveforms. The voltage balance between the flying capacitors of each level is illustrated in Fig. 7.

The load currents are given in Fig. 8. Each phase is loaded with 3 A of reactive current and phase A has an additional loading of 20 A of active current while the loads on phases B and C absorb no real power. These currents result in negative-sequence current component of 9.4 A and zero-sequence current component of 9.4 A.

The steady-state behavior of the MVUCSC phase currents is shown in Fig. 9. These currents are unbalanced and out of phase such that the upstream currents are balanced. The resulting substation currents are in Fig. 10. The neutral current seen by the substation has been reduced to effectively zero reflecting a reduction of the zero-sequence current to a negligible value. The negative sequence current has also been reduced to negligible values.

An FFT of the output current of the MV-UCSC is given in Fig. 11 showing that the converter as designed has a THD less than 5% at 100% of the designed current rating meeting the overall total-demand-distortion (TDD) requirements for grid-connected equipment from IEEE 1547-2003 [24]. The height of each bar in the FFT represents the peak value.

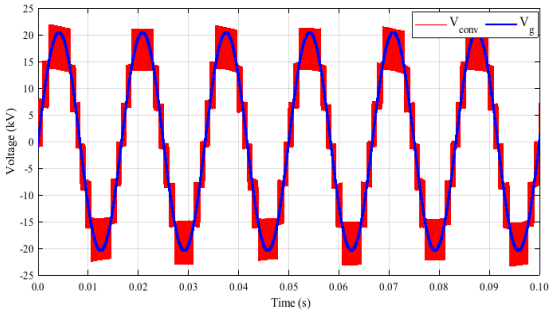

Fig. 6. Grid and converter output voltage line-to neutral during MV-UCSC compensation.

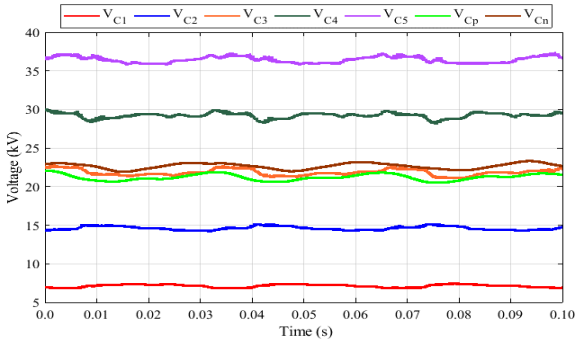

Fig. 7. Steady-state flying capacitor voltages during MV-UCSC compensation.

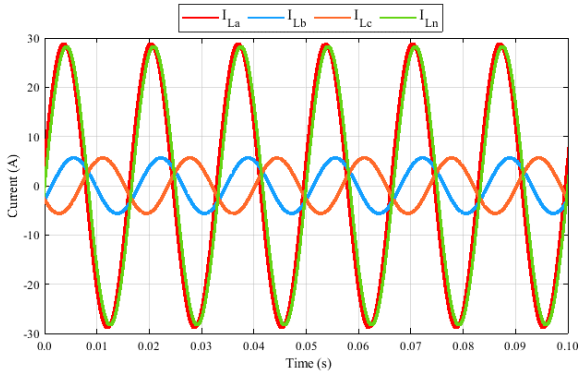

Fig. 8. Load currents during MV-UCSC compensation.

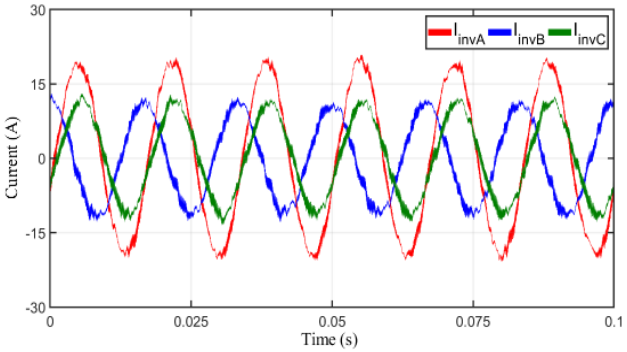

Fig. 9. Steady-state currents of the MV-UCSC during MV-UCSC compensation.

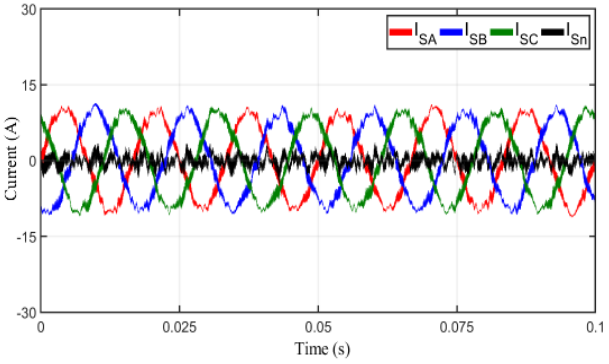

Fig. 10. Steady-state substation currents during MV-UCSC compensation.

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VI. Conclusions and Future Work

The proposed MV-FCC was designed based on the selection of the power modules to meet the required specifications. The switching frequency of these modules affected the designs of the FC unit and output LCL filter. The dc-bus capacitance was designed to withstand the high dc voltage and be able to transfer the power between all three phases for the MV-UCSC application. Selection of off-the-shelf component parts showed the feasibility of fabricating MV-UCSC. Furthermore, the power losses of the switching modules were evaluated to verify the selection of the 10-kV SiC MOSFET modules. The simulations validated the effectiveness of MV-UCSC by mitigating both negative- and zero-sequence currents and reducing the neutral current. The losses of passive power stage elements would be investigated deeply in future works and other functions could be performed using the proposed MV-UCSC.

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References

[1] A. P. S. Meliopoulos, J. Kennedy, C. A. Nucci, A. Borghetti and G. Contaxis, "Power distribution practices in USA and Europe: impact on power quality," 8th International Conference on Harmonics and Quality of Power. Proceedings (Cat. No.98EX227), pp. 24-29 vol.1, 1998.

[2] R. G. Harley, E. B. Makram, and E. G. Duran, "The effects of unbalanced networks on synchronous and asynchronous machine transient stability," Electric Power System Research, vol. 13, pp. 119-127, Oct. 1987.

[3] V. Jones, J. C. Balda and R. Adapa, "Current Compensators for Unbalanced Electric Distribution Systems," 2018 IEEE Electronic Power Grid (eGrid), 2018, pp. 1-6, doi: 10.1109/eGRID.2018.8598659.

[4] R. H. Salim, R. A. Ramos, and N. G. Bretas, "Analysis of the small signal dynamic performance of synchronous generators under unbalanced operating conditions," in IEEE PES General Meeting, 2010, pp. 1-6.

[5] B. N. Gafford, W. C. Duesterhoeft, and C. C. Mosher, "Heating of Induction Motors on Unbalanced Voltages," Transactions of the American Institute of Electrical Engineers. Part III: Power Apparatus and Systems, vol. 78, no. 3, pp. 282-286, 1959.

[6] T. A. Short, Electrical Power Distribution Handbook. Boca Raton, FL: CRC Press Taylor & Taylor Group, 2004.

[7] R. M. C. L.F. Ochoa, A. Padilha-Feltrin, G.P. Harrison, "Evaluation of distribution system losses due to load unbalance," presented at the 15th Power Systems Computation Conference PSCC 2005, Liège, Belgium.

[8] T. H. Chen, "Evaluation of line loss under load unbalance using the complex unbalance factor," IEE Proceedings - Generation, Transmission and Distribution, vol. 142, no. 2, pp. 173-178, 1995.

[9] T. U. Okeke and R. G. Zaher, "Flexible AC Transmission Systems (FACTS)," 2013 International Conference on New Concepts in Smart Cities: Fostering Public and Private Alliances (SmartMILE), 2013.

[10] G. R. F. Q. Mafra, W. Uturbey and B. J. Cardoso Filho, "Analysis of the operation of a D-STATCOM in unbalanced distribution systems under Conference and Exposition: Latin America (T&D-LA), Sao Paulo, 2010.

[11] G. F. Reed et al., "Application of a 5 MVA, 4.16 kV D-STATCOM system for voltage flicker compensation at Seattle Iron and Metals," 2000 Power Engineering Society Summer Meeting (Cat. No.00CH37134), Seattle, WA, 2000, pp. 1605-1611 vol. 3.

[12] M. Barghi Latran, A. Teke and Y. Yoldaş, "Mitigation of power quality problems using distribution static synchronous compensator: a comprehensive review," IET Power Electronics, vol. 8, no. 7, pp. 1312-1328, 7 2015.

[13] J. Rodriguez et al., "Multilevel Converters: An Enabling Technology for High-Power Applications," in Proceedings of the IEEE, vol. 97, no. 11, pp. 1786-1817, Nov. 2009, doi: 10.1109/JPROC.2009.2030235.

[14] S. Ji, Z. Zhang and F. Wang, "Overview of high voltage sic power semiconductor devices: development and application," in CES Transactions on Electrical Machines and Systems, vol. 1, no. 3, pp. 254-264, September 2017, doi: 10.23919/TEMS.2017.8086104.

[15] G. I. Orfanoudakis, M. A. Yuratich, and S. M. Sharkh, "Analysis of dc-link capacitor current in three-level neutral point clamped and cascaded H-bridge inverters," IET P. Electronics, vol. 6, no. 7, pp. 1376-1389, 2013.

[16] S. Qin, Y. Lei, Z. Ye, D. Chou and R. C. N. Pilawa-Podgurski, "A High-Power-Density Power Factor Correction Front End Based on Seven-Level Flying Capacitor Multilevel Converter," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 3, pp. 1883-1898, Sept. 2019, doi: 10.1109/JESTPE.2018.2865597.

[17] D. Jiao, Q. Huang and A. Q. Huang, "Evaluation of Medium Voltage SiC Flying Capacitor Converter and Modular Multilevel Converter," 2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, 2020, pp. 4386-4392, doi: 10.1109/ECCE44975.2020.9235758.

[18] J. W. Palmour et al., "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Waikoloa, HI, 2014, pp. 79-82, doi: 10.1109/ISPSD.2014.6855980.

[19] B. Passmore et al., "The next generation of high voltage (10 kV) silicon carbide power modules," 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, 2016.

[20] J. Hayes et al., "Dynamic Characterization of Next Generation Medium Voltage (3.3 kV, 10 kV) Silicon Carbide Power Modules," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2017, pp. 1-7.

[21] G. G. Oggier, R. G. Jimenez, Y. Zhao and J. C. Balda, "Modeling and Characterization of 10-kV SiC MOSFET Modules for Medium-Voltage Distribution Systems," 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Dubrovnik, Croatia, 2020, pp. 583-590.

[22] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil and S. Bhattacharya, "Design Considerations and Development of an Innovative Gate Driver for Medium-Voltage Power Devices With High dv/dt," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5256-5267, June 2019.

[23] Y. Sato, M. Iimura, Y. Dodo, and H. Obara, "A study on minimum required capacitance in flying capacitor multilevel converters for grid-connected applications," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 3502-3507.

[24] A. Reznik, M. G. Simões, A. Al-Durra, and S. M. Muyeen, "LCL Filter Design and Performance Analysis for Grid-Interconnected Systems," IEEE Transactions on Industry Applications, vol. 50, no. 2, pp. 1225-1232, 2014.

[25] A. Lachichi, A. Junyent-Ferre and T. Green, "Optimal Design of a LCL Filter for LV Modular Multilevel Converters in Hybrid AC/DC Microgrids Application," IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, 2018, pp. 3973-3978.

[26] W. Wu, Y. He, T. Tang and F. Blaabjerg, "A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter," in IEEE Transactions on Industrial Electronics, vol. 60, no. 10, pp. 4339-4350, Oct. 2013, doi: 10.1109/TIE.2012.2217725.

[27] Insulation coordination for equipment within low-voltage systems IEC/CEI 60664-1:2007.

[28] V. Dargahi, A. Khoshkbar-Sadigh and K. Corzine, "Analytic determination of conduction power losses in flying capacitor multicell power converter," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 2358-2364.

[29] O. J. K. Oghorada and L. Zhang, "Performance evaluation of pulse width modulation techniques for losses reduction in modular multilevel flying capacitor converter," 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), 2016, pp. 1-6.

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