Prof. Ramachandra Achar, Ph. D., P. Eng., IEEE Fellow
Professor, Department of Electronics,
Carleton University, Ottawa, Ontario - K1S 5B6
Email: achar@doe.carleton.ca
URL: www.doe.carleton.ca/~achar
Ph: 613-520-5651, Fax: 613-520-5708

EMCS DL Topics

1) Demystifying Signal Integrity in High-Speed Designs

With the increasing demands for higher signal speeds coupled with the need for decreasing feature sizes, signal integrity effects such as delay, distortion, reflections, crosstalk, ground bounce and electromagnetic interference have become the dominant factors limiting the performance of high-speed systems. These effects can be diverse and can seriously impact the design performance at all hierarchical levels including integrated circuits, printed circuit boards, multi-chip modules and backplanes. If not considered during the design stage, signal integrity effects can cause failed designs. Since extra iterations in the design cycle are costly, accurate prediction of these effects is a necessity in high-speed designs. Consequently, preserving signal integrity has become one of the most challenging tasks facing designers of modern multifunction and miniature electronic circuits and systems. This talk provides a comprehensive approach for understanding the multidisciplinary problem of signal integrity: issues/modeling/analysis in high-speed designs.

2) Advanced Modeling and Simulation Strategies for Power Integrity in High-Speed Designs

Preserving power integrity has become one of the most challenging tasks facing designers of modern multifunction and miniature electronic products. As devices scale and more transistors are integrated into a single integrated circuit, the power and current levels are expected to increase with a corresponding decrease in voltage. With gigabit signals being propagated through the package and board, the ability to supply clean power to the transistor circuits becomes very critical. Voltage variations may lead to reduced noise margins and may increase propagation delays. Reduced noise margins can cause false switching of gates whereas increased delays may lead to timing errors and impede the overall operating speed of the chip. These issues make the design of robust and reliable power distribution networks (PDNs),

consisting of chips, packages and printed circuit boards, essential to the success of the high-speed and high-density products. This talk provides an integrated approach for understanding power integrity issues and their modeling/analysis in modern low power, high-speed and multifunction designs.

3) Macrmodeling for Mixed-Domain Analysis of Multi-Physics Issues in High-Speed Designs

Massive evolution that is taking place in the global high-technology industry has made the electronics, computing and communications products to be part of day-to-day life and highly pervasive. From the user's end, there is an enormous demand for low-power, faster and multi-function designs. However, such a mandate warrants mixed-domain analysis of multi-physics issues of signal/power/EMI, involving very large sets of circuit equations. Model-order reduction (MOR) based techniques, such as Asymptotic Waveform Evaluation (AWE), CFH (Complex Frequency Hopping) and Krylov based projection techniques have emerged as effective tools to address this issue, in the recent years. Also vector-fitting based macromodeling approaches have been very successful in synthesizing circuit models from the given tabulated data. In this talk, fundamentals as well as advances of model-order reduction and macromodeling techniques will be covered. Particular emphasis will be made on physical properties of the models, such as passivity and causality, and their applications to signal/power/EMI analysis.