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A Modular Switching Position with Voltage-Balancing and Self-Powering for Series Device Connection

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***Abstract*- Medium-voltage converters, especially those making use of SiC devices, require high common-mode voltage immunity and resilience against associated high dv/dt across multiple isolation barriers. A truly modular and common-mode immune switching position could be beneficial for these applications. The design of a modular switching position is presented here for series connection of power semiconductors with voltage-balancing and self-powered-gate capabilities. The designs of the voltage-balancing and self-powered circuits are described followed by simulations and testing of a 3.3-kV switching position formed by two 1.7-kV SiC MOSFETs in series. Testing results demonstrate the ability of the proposed switching position to balance the voltage across series-connected MOSFETs even if the gate signals of the series-connected devices are not perfectly synchronized, while powering themselves directly from the OFF-state voltage across them. Additionally, a start-up circuit for the switching position is proposed and experimentally confirmed.**

I. Introduction

Continued advances in high-voltage SiC devices, and the move towards medium-voltage converters with multilevel topologies using these devices, call for a truly modular switching position. In this paper a switching position is defined as a power semiconductor device used in the primary power processing of a converter along with all the associated circuitry required for this device's operation. Connecting devices in series to realize a high-voltage switching position can make it possible to increase the switching frequency and reduce the position on-state voltage drops at the expense of higher complexity [1, 2]. Such a switching position requires mitigation of the common-mode current issues for power and control signals [3]. It also requires compensation for imperfect static and dynamic voltage sharing between series-connected devices [1].

Traditional methods by which the gate driver power supplies are designed becomes a challenge at medium-voltage levels (e.g., 13.8 kV) because the isolation required can be greater than 25 kV and may need to withstand dv/dt's across this isolation barrier greater than 100 kV/μs. This performance requires careful design of galvanically isolated power supplies and sometimes non-traditional supply configurations that can result in large and expensive solutions.

This problem has been reported extensively in literature [3-5]. Power-over-fiber (POF) systems can be used but these are large and relatively inefficient [6, 7]. Photonically-switched power devices have also been explored, but this does not provide power for any diagnostic circuitry surrounding the device [8]. Reference [9] proposes a bootstrapping method to provide power to all upper devices in a stack by using a single power supply on the lower switch. This method removes the need for a power supply at each power device for gating but doesn't eliminate the common-mode parasitic current paths due to the bootstrap diode capacitances. Inductive power transfer for power switch positions is used in [10] with an emphasis on low cost and reliability. The drawback for this method is low efficiency as the distance between primary and secondary windings increases and thus requires an optimization between efficiency and insulation/size.

Self-powered gate driver topologies have been suggested in [11-13]. This allows for the removal of the common-mode voltage issue with optical isolation being used for control signals. Reference [11] uses the natural switching of the power device to provide power by pairing a resonant circuit with a resonant gate-drive to minimize the power consumption. However, the resonant gate-drive may not be suited for active gate control as discusses below. A linear-regulator-based self-powered mechanism is proposed in [12] which has low efficiency, but its snubber-like properties can be used to decrease switching losses.

The most obvious power solution for a modular switching position would be to place an external high step-down commercial power supply across each power device along with a snubber which acts as an input filter. Such a setup is suggested in [14]. The drawback is the constant-power-load nature of an off-the-shelf power supply which may contribute to static voltage imbalance between devices in a leg. Therefore, that work suggests a compensating algorithm to overcome this effect, though this requires voltage sensing of the input filter for each power supply in a stack. A similar solution is given in [15] for a modular multilevel converter (MMC) building block with self-powering. This type of solution is elegant for the MMC but can suffer from the same constant-power load problem due to the local feedback mechanism and extrapolation of the solution to other converter applications is not obvious.

This paper is an extension of "A Hybrid Snubber for Voltage-Balancing and Self-Powering of Series-Connected Devices," presented at IEEE APEC 2019.

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References [1, 2, 16-21] proposed several different voltage-balancing circuits for connecting devices in series. Passive snubber circuits was used in [2] to form a 6.5-kV SiC MOSFET switching position with four series-connected 1.7-kV SiC MOSFETs. A super-cascode configuration SiC JFETs to form a 5kV switch was explored in [22] and SiC MOSFETs were used to form a 7.2 kV switch in [23]. These can provide low on-resistance and fast switching times, but commercially are still limited to relatively low voltages.

A quasi-active gate control is introduced in [21] which uses balancing resistors and bootstraps a low-side gate signal to trigger all devices in a stack and ensure similar gate signal. Though the circuit is simple it requires care to design against circuit resonances and provides a common-mode current path through the RC networks to the gate drive circuitry. Similar solutions are presented in [24, 25].

An active gate driver with an FPGA-based closed-loop gate-current controller in [16] adjusts the switching speeds based on the voltage detected across the power switch. Reference [17] presented a similar solution but using an analog feedback mechanism rather than digital. This sort of feedback requires clean on-board voltage measurements and may be susceptible to excess delays.

A resonant network with coupled inductors is presented in [18] for voltage balancing two series-connected devices. Reference [19] suggests using coupled inductors to guarantee the same gate pulses. The drawbacks are the introduction of leakage or parasitic inductance into the gate path, and the economics of custom transformer design for each application.

Voltage balancing, loss minimization, and modularization were the focus of [26] which suggests a resonant snubber that is clamped by a voltage source paired with a gate signal sharing network. The disadvantages involve the introduction of an extra series inductance in the load current path, and the "daisy chain" constructed for the gate signals that may decrease the switch fault resiliency of a stack of power devices.

Reference [27] uses an open-loop active circuit to inject current into the gate when an overvoltage condition occurs. The active component of this circuit allows for low losses when the voltages are balanced but additional semiconductors may make the circuit less reliable. In an attempt to make a completely modular and "stackable" switching position, [27] suggested a combination of a self-powered circuit and a voltage-balancing circuit. To achieve the goal of a fully modular switching position with low part count, simple control and soft-start capability, a combination of a modified configuration of the voltage balancing circuit in [1] so this approach could be used in multilevel converters, and a new built-in self-powered circuit is proposed in this paper building from the work presented in [28]. In particular, the following new contributions.

A procedure for determining the component values of the voltage-balancing circuit for inductive loading is shown and an analysis of its use in half-bridge circuits. A new soft-start circuit that takes advantage of the used components to reduce part count is proposed to provide power to the switch when the voltage across it is much lower than nominal value. Lastly, a method for pre-charging the voltage-balancing circuitry by taking advantage of this newly presented start-up circuit for half-bridge applications is shown.

The paper is structured as follows: The proposed switching position is described in Section II. A novel design methodology for determining the components for the voltage-balancing circuit is given in Section III. Defining equations for design of the self-powered circuitry are addressed in Section IV. The novel start-up configuration is given in Section V. Simulation results for the circuit designs are illustrated in Section VI and experimental results are evaluated in Section VII. An appendix provides a design example.

II. The Proposed Modular Switching Position

The circuit configuration of the proposed modular switching position is given in Fig. 1. The function of the voltage-balancing circuit is to ensure dynamic and static voltage balance between series connected devices. The built-in self-powered gate circuit uses the switching of the power semiconductor device to provide power to the gate and other auxiliary circuitry. These two circuits are shown across a power semiconductor device along with a simple gate driver circuit.

All that is needed to interface with the switching position is the gate signal fiber optic cabling, making it ideal for use in multilevel converters in which size, common-mode voltage and dv/dt immunity are problematic. Just one switching position would be designed for the required current and voltage ratings of a more-readily-available power semiconductor device and then simply stacked to achieve the desired voltage rating. The voltage-balancing circuit and the built-in self-powered circuit are not involved in processing the *main* power flowing through the switching position.

From Fig. 1, the proposed voltage-balancing circuit requires only passive components and diodes. This can be compared to the common series-connection approach from [2]. That approach uses RC snubbers to keep the voltages dynamically and statically balanced. The use of these snubbers is proven to be effective, but unfortunately, these circuits can cause additional static and switching losses in the circuit. The voltage-balancing circuit in this paper avoids these losses because it can have very little static losses and does not contribute much to switching losses.

The self-powered circuit replaces the high-voltage-transient immune power supply and all the associated magnetics and components [7]. All of these circuits' components could be integrated into a singular module like it is done in typical commercially available isolated power supplies. So, the commercial power supplies should not be considered a singular component when making comparisons. And, unlike the traditional external power supplies, the built-in self-powered structure does not require an increase in size or a change in isolation material as the common-mode voltage of the application increases. Only a change in the voltage across the switch S or current rating would require a redesign. In summary, the proposed solution allows for reaching higher converter voltages more easily and could contribute to the reduction in size of the converter cabinet.

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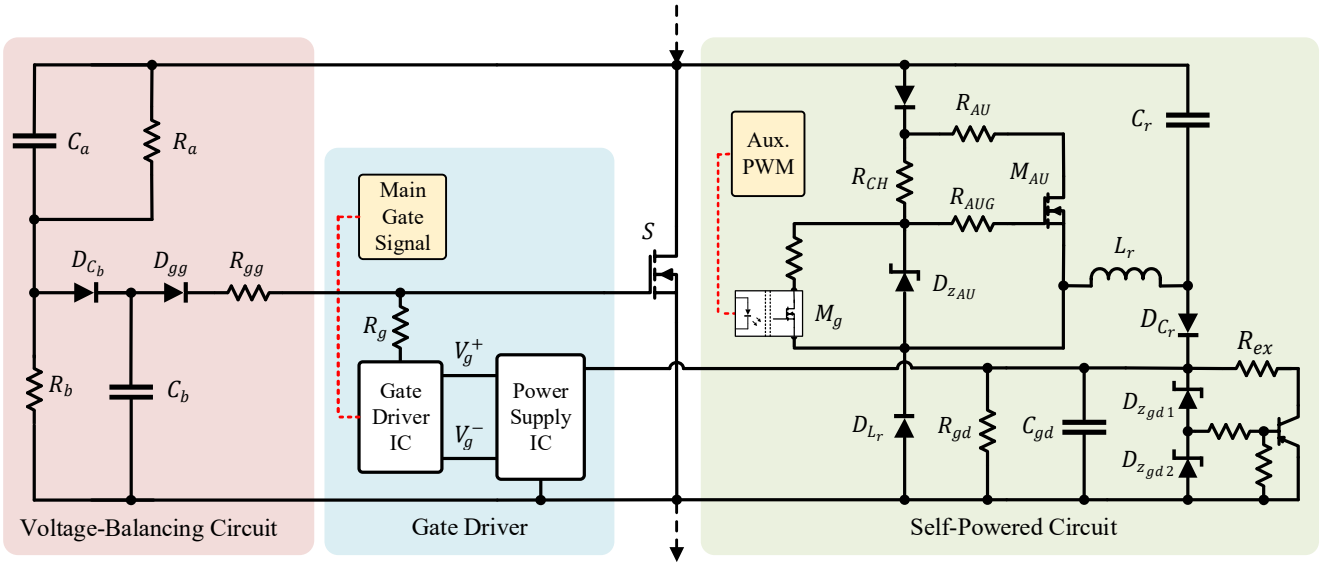

Fig. 1. The proposed modular switching position.

III. Design Methodology for the Voltage-Balancing Circuitry

The voltage-balancing circuit in [1] was modified so it could be operated as a half bridge (e.g., the addition of diode D_{C_b}). The modifications and the reasoning behind it are given in subsection III.C. A switch S from a stack of series-connected switching positions is shown with the voltage-balancing circuit in Fig. 2. Resistances R_a and R_b maintain the static balancing of the voltage between each switch position in the stack. However, this is not adequate during switching transients, so capacitors C_a and C_b are added to provide dynamic voltage-balancing.

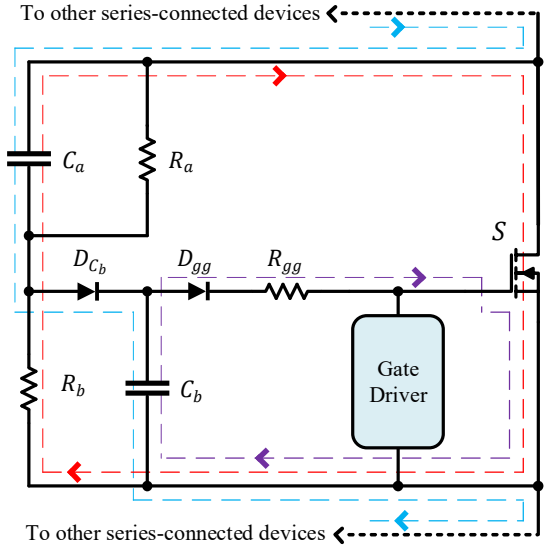

Fig. 2. The voltage-balancing circuit across a power device.

Under normal operation C_a is charged to the nominal OFF-state voltage, V_S, of S. Because $C_a >> C_b$, any excess voltage when the voltage across S rises sharply will appear mostly across C_b. This current path is shown in blue. Simultaneously, the voltage across C_b results in a current, shown in purple, into the gate of the power device, S, which charges its gate capacitance, C_g, and begins to turn the device ON. This mechanism protects S from overvoltage events that occur when one or more devices in a stack of devices turns ON before S (or when S turns-OFF before the others). Excess energy that may be accrued by C_a during a compensation event is expended by R_b when S is ON. This current path is shown red.

Though the basis for the circuit was suggested in [1], only a "rule-of-thumb" process for selecting the component values was given. The following two subsections present a new methodology for choosing the components for the voltage-balancing circuit with resistive [28] and also current-source (charged inductor) loadings. In addition, the modification to the voltage-balancing circuit from [1] and the reasoning behind it are given in a third subsection.

Consider that switches $S1$ and $S2$ in Fig. 3 are initially OFF and have balanced voltages across them. Assume that $S1$ begins to turn-ON before $S2$. The voltage across $C_{a_{S2}}$ is V_S, and $C_{a_{S2}} >> C_{b_{S2}}$, so as the voltage across $S2$, $V_{DS_{S2}}$, begins to increase almost all of this voltage increase appears across $C_{b_{S2}}$. This charges the gate capacitance of $S2$, $C_{g_{S2}}$, turning $S2$ ON before it is destroyed.

The design process developed here assumes a worst-case scenario in which the gate pulse offset, t_{off}, between $S1$ and $S2$ is larger than the turn-ON time of $S1$ and the turn-OFF time of $S2$ combined. This means that $S1$ can completely turn ON before $S2$ begins to turn ON. It is expected that t_{off} is normally much smaller.

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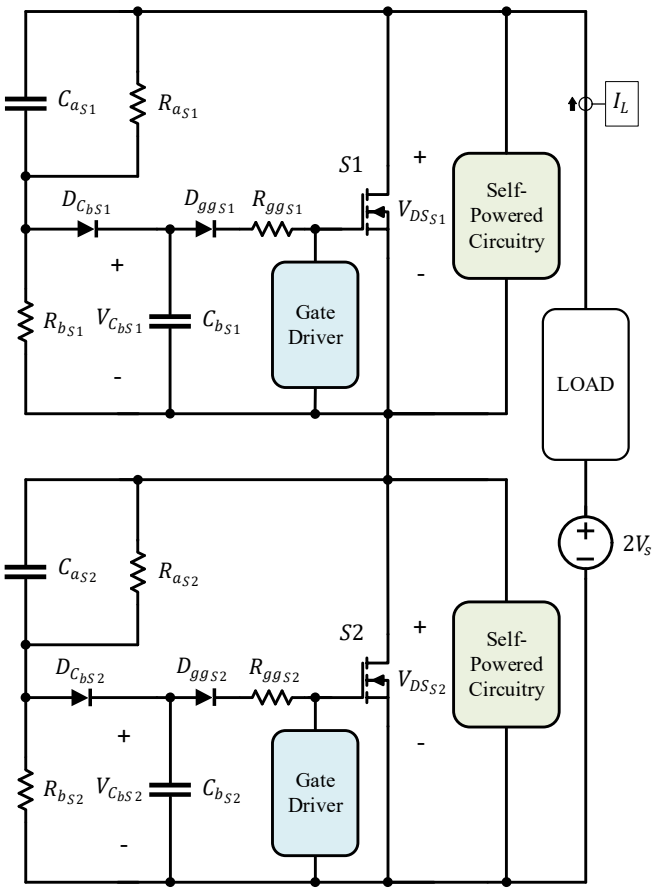

Fig. 3. A series connection of two modular switching positions.

The processes below give a starting point for selecting the component parameters for $S2$ and thus $S1$, since they are identical. So, the "2" subscript is removed when applicable.

A. Resistive Loading Conditions

The process for choosing the component values is as follows:

1) Design the gate drive using normal methods [29-31]. This determines R_g, V_g^+, V_g^-.

2) Choose the maximum voltage overshoot, ΔV_{DS}, for the switch S. Then the resistance R_{gg} is calculated by

$$R_{gg} < \frac{\Delta V_{DS} R_g}{V_{g,on} - V_g^-} \tag{1}$$

where $V_{g,on}$ is the gate voltage at which the device begins to turn ON (approximated from the datasheet), R_g is the gate resistance and V_g^- is the designed OFF-state gate voltage from Step 1.

3) Determine the dynamic behavior of C_b and C_g. The voltages V_{C_b} and V_{C_g} across C_b and C_g, are respectively defined in the Laplace domain as follows:

$$V_{C_b}(s) = \left(\frac{N_1}{D_1}\right)[V(s) - V_2(s)] + V_2(s), \tag{2}$$

$$N_1 = C_g R_g R_{gg} s + R_g + R_{gg}\,, \tag{3}$$

$$D_1 = C_b C_g R_L R_g R_{gg} s^2 + \ldots \ldots R_L(R_g + R_{gg})(C_b + C_g)s + R_L + R_g + R_{gg}, \tag{4}$$

$$V_2(s) = \frac{N_2}{D_2}, \tag{5}$$

$$N_2 = R_g R_{gg} C_b C_g V_{C_b}(0)s^2 + R_g C_b V_{C_b}(0)s \ldots + R_g C_g V_{C_g}(0)s + R_{gg} C_b V_{C_b}(0)s + V_g^-\,, \tag{6}$$

$$D_2 = s\left(R_g R_{gg} C_b C_g s^2 + R_g C_b s + \ldots \ldots R_g C_g s + R_{gg} C_b s + 1\right), \tag{7}$$

$$V_{C_g}(s) = \left(\frac{R_g}{C_g R_g R_{gg} s + R_g + R_{gg}}\right) \ldots \ldots \left[V_{C_b}(s) - V_1(s)\right] + V_1(s)\,, \tag{8}$$

$$V_1(s) = \frac{R_g C_g V_{C_g}(0)s + V_g^-}{R_g C_g s^2 + s}, \tag{9}$$

with $V_{C_b}(0)$ and $V_{C_g}(0)$ as initial conditions, and R_L and R_g as the load and gate resistances. Capacitor C_g is approximated by the C_{ISS} specified in the datasheet for switches $S1$ and $S2$.

The equivalent circuit for voltage-balancing action with a resistive load is drawn in Fig. 4. The voltage drops across the diodes are neglected. The compensation event can be divided into three periods or "modes." A piecewise approximation of the compensation event can be constructed using the inverse Laplace transformation of (2) and (8) during each mode.

MODE I begins when $S1$ begins to turn ON before $S2$. Both C_b and C_g begin to charge, but V_{C_g} remains below $V_{g,on}$. Voltage $V(s)$ from (2) is given in the Laplace domain as

$$V(s) = \frac{V_S}{t_r s^2} \tag{10}$$

where t_r is the fall time of the device.

MODE II begins after t_r has elapsed. Capacitors C_b and C_g are still charging and V_{C_g} remains below $V_{g,on}$. However, $V(s)$

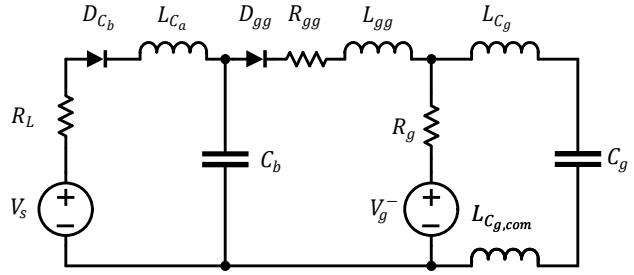

Fig. 4. Equivalent circuit for voltage-balancing action with resistive load.

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from (2) is now given by:

$$V(s) = \frac{V_S}{s} \tag{11}$$

because $S1$ is fully ON.

MODE III begins once $V_{C_g} = V_{g,on}$. Capacitor C_b is no longer charging because $S2$ has begun to turn ON, the voltage across C_a prevents any further charging of C_b and $V(s)$ from (2) is then

$$V(s) = V_2(s) \tag{12}$$

so that the first term in (2) is zero. Capacitor C_g may continue to accrue charge for a time because C_b is discharging into it. It then discharges into C_g and the gate drive.

Table I describes each of the three modes I-III of the compensation action for a resistive load including the value of $V(s)$ from (2) during each mode and their durations. The modes occur in order. The time $t_{V_g=V_{g,on}}$ is at which $V_g = V_{g,on}$. And $t_{MODE\ II}$ is the time when MODE II ends. The theoretical waveforms for these modes are shown in Fig. 5.

4) Choose C_b such that the circuit is operating in MODE III when $S2$'s gate driver begins to apply its ON-state voltage.

Capacitor C_a is then chosen to be $100C_b$. Resistance R_a can be chosen as a static balancing resistance for the switching position if needed. Using a shunt resistance like R_a to compensate for leakage current mismatch is a well-known subject and is not covered in this paper [32].

5) Calculate the extra energy, ΔE_{C_a}, that is absorbed by C_a. This energy needs to be removed, otherwise V_{C_a} will become

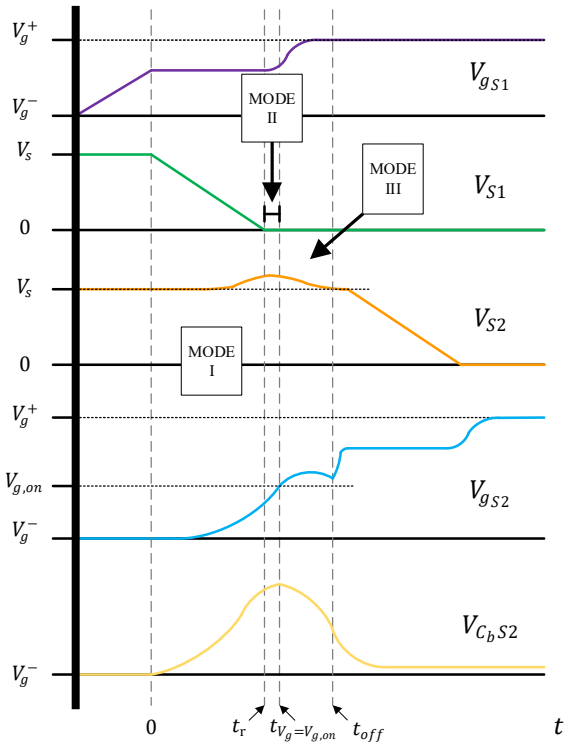

Fig. 5. Theoretical waveforms for resistive loading.

TABLE I
VALUES OF *V(S)* DURING EACH MODE

RESISTIVE LOADING					
MODE	$V_{Cg} > V_{g,on}$ [a]	C_b [b]	C_g [b]	$V(s)$	Duration
I	X	+	+	$\frac{V_S}{t_r s^2}$	t_r
II	X	+	+	$\frac{V_S}{s}$	$t_{V_g=V_{g,on}} - t_r$
III	✓	-	+ or -	$V_2(s)$	$t_{off} - t_{MODE\ II}$

CURRENT SOURCE LOADING					
MODE	$V_{Cg} > V_{g,ss}$ [a]	C_b [b]	C_g [b]	$I_l(s)$	Duration
I	x	+	+	$\frac{I_L}{t_r s^2}$	$t_{V_g=V_{g,on}}$
II	✓	- or =	- or =	$\frac{V_{C_b,ss} + V_g^-}{s(R_{gg} + R_g)}$	$t_{off} - t_{MODE\ I}$

[a] Indicates if the given condition is TRUE (✓) or FALSE (x)
[b] Indicates if the given capacitance is charging (+) or discharging (-) or remaining the same (=)

unbalanced for as long as $|t_{off}| > 0$. Resistance R_b should be chosen such that this energy is drained from C_a when $S2$ is ON. ΔE_{C_a} is determined from the current into C_a during the compensation event (the blue path in Fig. 2). ΔE_{C_a} from each event can be integrated over a period to give an equivalent power P_{C_a} that R_b should dissipate. For a constant switching frequency, f_{sw}, this power is defined as

$$P_{C_a} = \Delta E_{C_{a,avg}} f_{sw} \tag{13}$$

where $\Delta E_{C_{a,avg}}$ is the average expected ΔE_{C_a}. With P_{C_a}, R_b can be chosen according to

$$R_b < \frac{V_s^2}{P_{C_a}} d_{avg} \tag{14}$$

d_{avg} is the average duty cycle applied to $S2$.

B. Current Source Loading Conditions

The process with a current-source load is as follows:

1) Follow Steps 1 and 2 from Section III.A

2) Determine the behavior of C_b and C_g. The voltage across C_b and the gate capacitance, C_g, are defined in the Laplace domain as

$$V_{C_b}(s) = \frac{N_3}{D_3} + I_1(s)\frac{N_4}{D_4}, \tag{15}$$

$$\begin{aligned} N_3 &= R_g R_{gg} C_b C_g V_{C_b}(0) s^2 + V_g^- + \ldots \\ &\ldots \left(C_b R_g V_{C_b}(0) + C_b R_{gg} V_{C_b}(0) + R_g C_g V_{C_g}(0)\right) s, \end{aligned} \tag{16}$$

$$\begin{aligned} D_3 &= R_g R_{gg} C_b C_g s^3 + \ldots \\ &\ldots \left(C_b R_g + C_b R_{gg} + C_b R_g\right) s^2 + s, \end{aligned} \tag{17}$$

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$$N_4 = \left(R_g + R_{gg} + C_g R_g R_{gg} s\right), \tag{18}$$

$$D_4 = C_b C_g R_g R_{gg} s^2 + \ldots \ldots \left(C_b R_g + C_b R_{gg} + C_g R_g\right) s + 1, \tag{19}$$

$$V_{C_g}(s) = \frac{V_g^- + C_g R_g V_{C_g}(0) s}{C_g R_g s^2 + s} + \ldots \ldots \frac{R_g\left(V_{C_b}(s) + \frac{V_g^- + C_g R_g V_{C_g}(0) s}{C_g R_g s^2 + s}\right)}{\left(R_{gg} C_g R_g s + 1 + R_g\right)}, \tag{20}$$

where I_1 from (15) is the current through D_{C_b}.

3) Determine the current balance between I_1 and the current through R_{S2}, $I_{R_{S2}}$. The equivalent circuit for the current-source load is illustrated in Fig. 6. Through device characterization, an equivalent resistance can be derived for switch $S2$ based on V_{C_g}. An equilibrium between the current going through the branch containing R_{gg} and the branch containing R_{S2} can be predicted based on this equivalent resistance. The relationship is defined by

$$I_L = \frac{V_{C_g,ss} - V_g^-}{R_g} + \frac{V_{C_b,ss} + V_S}{R_{S2}}, \tag{21}$$

$$R_{S2} = f\left(V_{C_g}\right), \tag{22}$$

where $V_{C_g,ss}$ and $V_{C_b,ss}$ are the steady-state values of v_{C_g} and v_{C_b}, at the end of the compensation event, respectively, and I_L is the load current. The compensation event can be divided into two periods or "modes." Like with the resistive loading, this can be used to form a piecewise function approximation of the compensation event by using the inverse Laplace transforms of (15) and (20)

MODE I begins when $S1$ starts to turn ON before $S2$. Both C_b and C_g begin to charge, but V_{C_g} remains below $V_{g,on}$. Current $I_1(s)$ from (15) is given in the Laplace domain as

$$I_1(s) = \frac{I_L}{t_r s^2}. \tag{23}$$

MODE II begins when $V_{C_g} = V_{g,on}$. Voltages v_{C_g} and v_{C_b} converge to $V_{C_g,ss}$ and $V_{C_b,ss}$ and stay there until the end of MODE II when the gate driver for $S2$ takes over after t_{off}. $I_1(s)$ from (15) for this mode is

$$I_1(s) = \frac{V_{C_b,ss} + V_g^-}{s\left(R_{gg} + R_g\right)}. \tag{24}$$

Values for R_{S2}, $V_{C_g,ss}$ and $V_{C_b,ss}$ can be calculated manually for the worst-case load current. Table I describes both of these modes of the compensation action for a current source load including the value of $I_1(s)$ from (15) during each mode and their durations. $t_{MODE\,I}$ is the time when MODE I ends. The theoretical waveforms for these modes are shown in Fig. 7.

4) Choosing I_L and t_{off} determine the value of C_b. Because of the low-pass RC network formed by $(R_{gg} + R_g)$ and C_g,

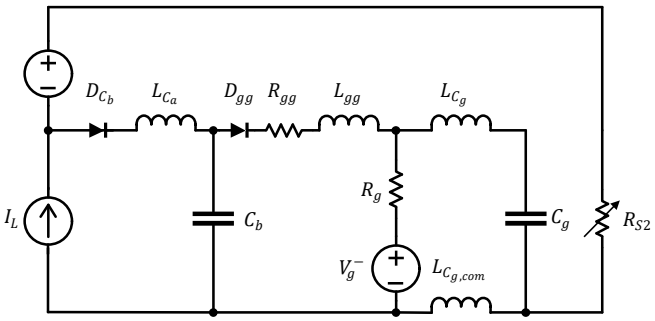

Fig. 6. Equivalent circuit for the voltage-balancing action with a current-source load.

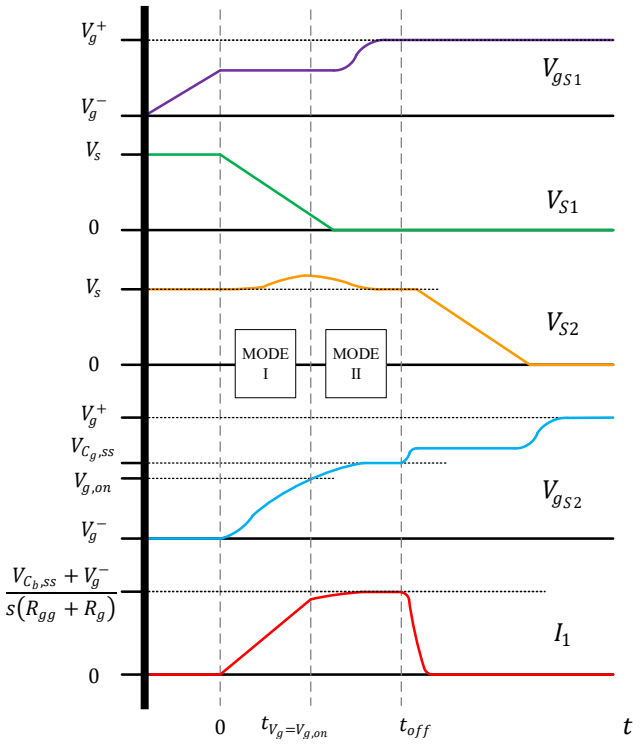

Fig. 7. Theoretical waveforms for a current-source load.

some overshoots above $V_{C_b,ss}$ and $V_{C_g,ss}$ may be experienced. This may lead to oscillations in v_{C_g} and thus in i_1.

From the inverse Laplace of (13)-(18) and the value of I_1 from Table I, choose a C_b value in which v_{C_b} is greater than $V_{C_b,ss}$ at the end of MODE I. Capacitance C_a is then chosen to be $100C_b$ and R_a can be chosen as a static balancing resistance for the switching position if needed.

5) Follow Steps 5 from Section III.A to determine R_b.

It is important to note that R_b will discharge C_a regardless of the value of t_{off}. This will result in a voltage drop on C_a that is dependent upon the time the switch is ON. When two of these modular switching positions are connected in a half-bridge configuration, a non-negligible charging current will be added to the load current experienced by each switching position

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during turn-ON, which will increase turn-ON losses. If t_{off} can be kept small, then the value of R_b can be increased and the reduction of V_{Ca} can be made negligible.

C. Voltage-Balancing Modification for Half-Bridge Operation

The effect of adding the voltage-balancing snubber from [1] needs to be evaluated for application in a half-bridge circuit. For simplicity only one of the proposed modular switching positions is used for the top and bottom switch locations, respectively. The addition of D_{C_bP} and D_{C_bN} is highlighted in green. Without D_{C_bP}, as is the case in [1], each time S_P turns ON it incurs additional losses associated with C_{bP} as it charges from 0 V to -$2V_S$ [33]. This current path is shown red with D_{ggP} blocking the reverse charge of the gate. The resulting power loss is defined as

$$P_{C_b} = \frac{1}{2} C_{bP} (2V_S)^2 f_{sw} \,, \tag{25}$$

with f_{sw} as the switching frequency of S_P.

Another source of losses comes from the discharge of C_{bP}. When S_P turns OFF, the load current, I_L, as indicated in Fig. 8 clamps the voltage across S_P to nearly 0 V by conducting through the anti-parallel diode. This keeps C_{bP} charged to -$2V_S$. When S_N turns ON after the switching deadtime capacitor C_{bP} will discharge into S_N resulting in additional turn-ON losses for S_N. This current path is shown in blue. The losses associated with this event are also given by (25).

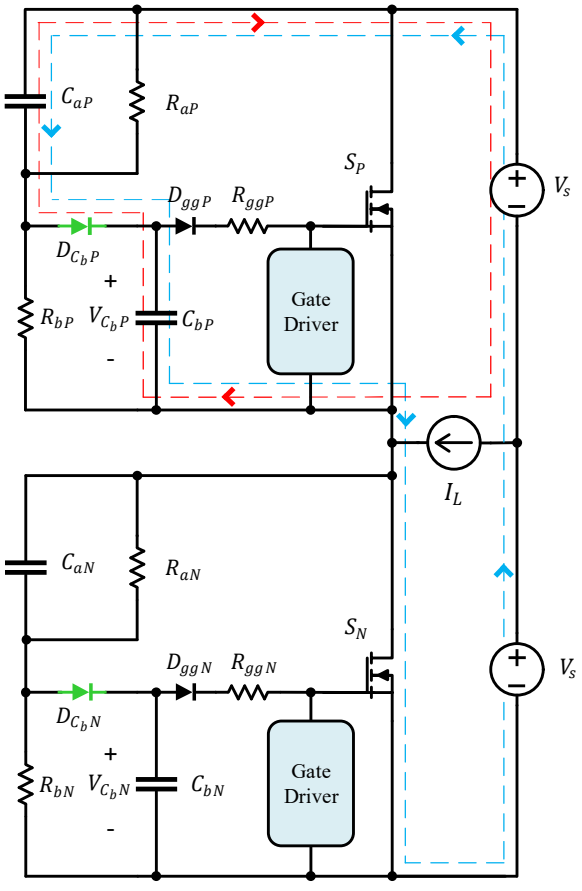

Fig. 8. The voltage-balancing circuit used in a half-bridge application.

With the introduction of D_{C_bP} and D_{C_bN} the path indicated in red is blocked for both switching positions so C_{bP} and C_{bN} can never be charged by C_{aP} and C_{aN}, respectively and thus, these loss sources are eliminated. Another advantage of D_{C_bP} and D_{C_bN} is that they clamp resonance between the voltage-balancing circuit capacitors and inductive elements in the path of the load current.

IV. Design Of The Self-Powered Circuitry

The circuit designed to power the gate driver using power drawn from across the power device is illustrated in Fig. 9. When the device S is OFF, capacitor C_r charges from -$V_{C_{gd}}$ to $\left(V_S - V_{C_{gd}}\right)$ through the blue current path shown in Fig. 9. Again, V_S is the expected OFF-state voltage across the MOSFET. This current also helps to charge C_{gd}. The energy delivered to C_{gd} is

$$E_1 = V_{C_{gd}} (C_r V_S) \,. \tag{26}$$

This charging current when used with resistive loading as in Fig. 3 is defined by

$$i_1(t) = \left(\frac{V_S}{R_L}\right) e^{-t/C_r R_L} \,, \tag{27}$$

$$t_{TOT1} \approx 5 C_r R_L \,, \tag{28}$$

where t_{TOT1} is the total amount of time to charge C_r. The current is constant when using a current-source load and the charging time is then givne by

$$t_{TOT2} = C_r \frac{V_S}{I_L} . \tag{29}$$

In (26) and (29) the assumption is that C_r is the only capacitance being charged. If there are other parallel capacitances across the switch S then the effect of this capacitive current divider must be included.

Upon turn-ON of S, the current resonates from C_r through L_r as shown in Fig. 9 in red. This current, i_{Lr1}, is defined by

$$i_{Lr1}(t) = \frac{V_{C_r} - V_{C_{gd}}}{\sqrt{\frac{L_r}{C_r} - \frac{R_{eq}^2}{4}}} e^{-\delta t} \sin(\omega t) \,, \tag{30}$$

$$\omega = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_{eq}}{2L_r}\right)^2} \,, \tag{31}$$

$$\delta = \frac{R_{eq}}{2L_r} \,, \tag{32}$$

where V_{C_r} is the voltage across C_r, $V_{C_{gd}}$ is the voltage across C_{gd}, and R_{eq} is the equivalent series resistance of the current path. The value of R_{eq} could be approximated using the dc

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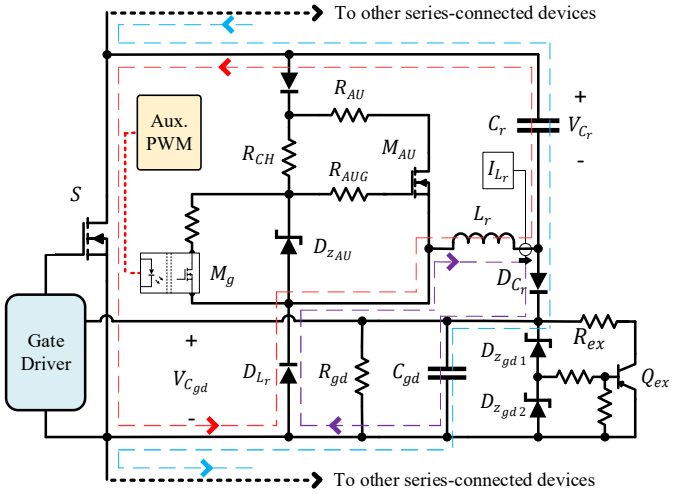

Fig. 9. Current commutations during the ON- and OFF-times of the power MOSFET.

resistances from the datasheet for each component involved in conducting the current (e.g., C_r, L_r, D_{L_r}). The current peak coincides with the discharging of C_r to 0 V, resulting in the total energy given by

$$E_2 = \frac{1}{2} L_r I_{pk1}^2 , \tag{33}$$

where I_{pk1}^2 is the peak value of i_{L_r1}. The peak occurs at

$$t_{pk1} = \frac{\tan^{-1}\left(\frac{\omega}{\delta}\right)}{\omega} . \tag{34}$$

After t_{pk1} the voltage across L_r reverses to maintain the flow of current and the energy in L_r then resonates into C_{gd} which is demonstrated in Fig. 9 in purple. This discharge slope is a function of $V_{C_{gd}}$ and L_r. The time needed to reduce the current through L_r to 0 (neglecting series resistance and voltage drop across D_{L_r} and D_{C_r}) is calculated by

$$t_{TOT3} = L_r \frac{I_{pk1}}{V_{C_{gd}}} . \tag{35}$$

The total power delivered to C_{gd}, P_T, is given by

$$P_T = \frac{1}{2}\left(E_2 - C_r V_{C_{gd}}^2 + E_1\right) f_{sw} . \tag{36}$$

Capacitor C_r is effectively in parallel with C_{gd} when the MOSFET is ON and thus the existence of the $C_r V_{C_{gd}}^2$ term in (33). The existence of the f_{sw} term in (36) means that a change in switching frequency causes a change in delivered power. This can allow P_T to scale up with the increased power needed by the gate driver circuitry, but considering the baseline power needed by the auxiliary/diagnostic circuitry of the switching position this relationship sets a lower limit for a frequency change. So this self-powered circuity is not effective in applications requiring always-ON operation of a device. Thus, this self-powered scheme is most useful in applications that do not require large variations in switching frequency.

Assuming a relatively low power consumption of the on-board circuitry, the value of C_r will be such that this resonant circuit does not contribute significantly to the turn-ON or conduction losses incurred by the switch upon which it is installed. However, C_r does contribute to the effective C_{OSS} of $S1$ and $S2$. This means that if C_r has a value comparable to C_{OSS} of $S1$ or $S2$, this can then contribute to the turn-ON losses when these modular switching positions are connected in a half-bridge configuration. Thus, there is a trade-off between the power supplied by the self-powered gate circuitry and the turn-ON losses in the devices, unless the charging current is otherwise limited, such as with a resistor in series with C_r.

As implied by the preceding analysis, this circuit, like the voltage balancing circuit, is required to support the entirety of the power device voltage. Depending on the voltage, this requires some relatively large clearance and creepage distances between components when using conventional PCB technology [34]. However, the intended application is to develop a higher density module that can be potted with an isolation material like it is done with commercial power supply modules.

V. Start-Up of the Switching Position

A. Overview

The switching position may not have power in some self-powered schemes until nominal voltage occurs across the switch, and thus any diagnostics that may be desirable for centralized control are inaccessible. Hence, special consideration needs to be given to the start-up procedure required in any application because the power for the switching position is derived from the voltage across the switch which will be at much lower than nominal at startup. To prevent this undesirable operating condition, the start-up circuit in Fig. 10 was added. In this configuration, L_r and its corresponding blocking diode are positioned to form a buck converter along with M_{AU} and C_{gd}.

Components M_{AU}, L_r, D_{L_r}, and C_{gd} are used as a buck converter to provide power to the switching position at all

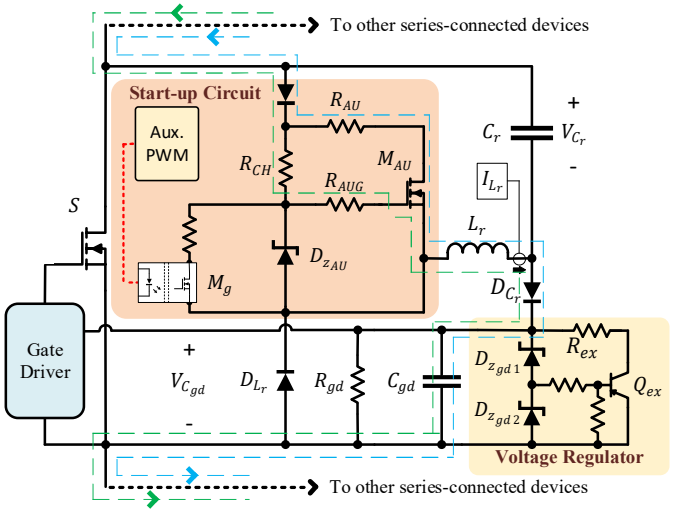

Fig. 10. Proposed modified self-powered circuit with start-up circuitry.

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voltages between the intended operating voltage of C_{gd}, $V^*_{C_{gd}}$, and V_S. The gate of M_{AU} is charged to the zener voltage of $D_{z_{AU}}$ through a large resistance value R_{CH}. This is the green current path. Switch M_g is used to modulate the voltage at the gate of M_{AU} according to a central controller. Through this bucking action, any diagnostics performed by the switching position are active starting slightly above $V^*_{C_{gd}}$, far below the nominal voltage V_S. Resistance R_{AU} remains as an initial current limiter as M_{AU} is in a "normally ON" configuration. The current path for the ON-time bucking action is shown in blue in Fig. 10. When M_{AU} turns-OFF the current path is identical to the purple path in Fig. 9.

Central/Identical duty cycle control of M_g for each switching position helps to keep the voltage balanced across each switch. The current paths in Fig. 10 indicate the dependency of each switching position on the ones above and below it. When the M_{AU} of a switching position is ON it depends on the M_{AU} in the adjacent switching positions to be ON as well. If each switching position was controlled independently, such as with an onboard voltage controller IC, they would operate as individual constant-power loads and possibly contribute to any voltage imbalance across the series-connected devices; so, this option was not selected.

To avoid any voltage imbalances that may occur from individual self-control of each switching position, the switching positions are controlled with a semi-open-loop central control method. From 0 V to 1.6 kV the required duty-cycle for this bucking mechanism is empirically determined at 10 V increments. The resultant Duty Cycle vs Switching Position Voltage curve from this characterization is presented in Fig. 11. This data is then broken into different sections and a curve fitting tool is used to fit curves to each section. From the individual curves a piecewise function is built into the start-up control that automatically adjusts the duty cycle for all switching positions based on the number of switching positions used and the total dc-bus voltage. The duty-cycle chosen at each increment can be chosen larger than required to compensate for any component parameter variation between different switching positions.

Instead of a simple Zener-diode-based regulator for C_{gd}, a Zener-BJT-based voltage regulator is used. This voltage regulator consists of $D_{z_{gd}1}$, $D_{z_{gd}2}$, R_{ex}, Q_{ex}, and small resistor network. Transistor Q_{ex} begins to turn-ON when $v_{C_{gd}}$ becomes greater than the breakdown voltage for D_{zgd1} plus the base-emitter voltage of Q_{ex}. This alleviates some of the current that would normally be shunted purely through the Zener diode. This allows for the selection of C_r for nominal bus voltage while allowing for voltage (and correspondingly power) swells across the power device to be dissipated by a more resilient power resistor. Or conversely, it is a simple way to lower the minimum operating voltage of the self-powered gate driver by oversizing C_r if the application requires operation during voltage sags.

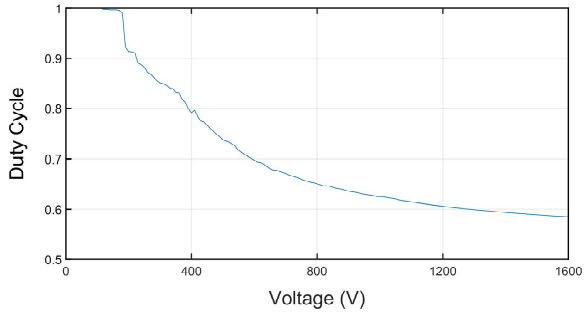

Fig. 11. Duty-cycle vs voltage for the start-up scheme.

B. Half-Bridge Operation

A basic half-bridge converter implemented with two modular switching positions is shown in Fig. 12, where the self-powered snubber circuit is neglected. The converter is connected to a resistive load through an LC filter. When the dc bus is initially charged to the nominal value, the voltages across C_{aP} and C_{aN}, $V_{C_{aP}}$ and $V_{C_{aN}}$ respectively, are half of the total bus voltage, $2V_S$. In fact, when S_P and S_N are not operating, the snubbers across

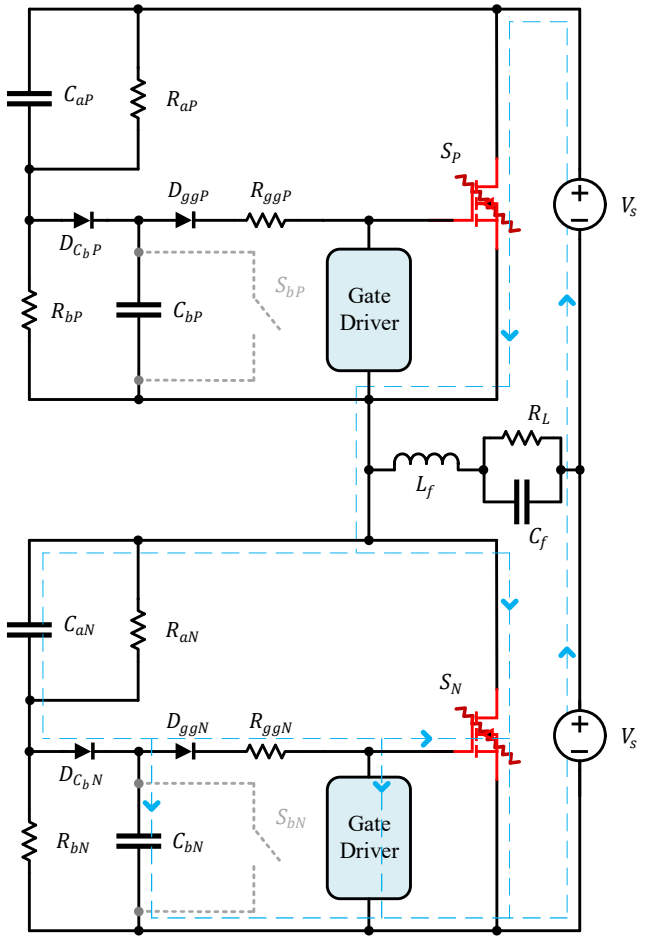

Fig. 12. Destructive start-up current path.

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both switches effectively form a resistor divider. This start-up condition presents two problems. When S_P turns ON, there is a charging current that goes through it, in addition to the load current. The current paths are shown in blue in Fig. 12.

The first problem is that a large positive dv/dt appearing across S_N can trigger the snubber balancing action. As a result, S_N could be forced ON causing a catastrophic shoot-through current event. Assuming some auxiliary switches S_{bP} and S_{bN} could be closed during this condition, the first problem can be avoided. However, this does not solve the following second problem. Due to the design requirements of the voltage-balancing snubber, the values of C_{aP} and C_{aN} will most likely far exceed the output capacitances of S_P and S_N. This means that S_P will be switching with a relatively large capacitive load, potentially resulting in a damaging overcurrent event.

Capacitors C_{aP} and C_{aN} must be charged to $2V_s$ before either S_P or S_N turn ON to avoid this condition. This can be achieved by utilizing the soft-starting capabilities of the self-powered snubber. When M_{auP} and M_{auN} are switched with the same pulses (in-phase), there is no net charge provided to C_{aP} or C_{aN} and the problem mentioned above persists. This is shown by the green path in Fig. 13(a). However, if the control pulses for M_{auP} and M_{auN} are offset (out-of-phase), this allows for the charging of C_{aP} and C_{aN} to nearly $2V_s$. The current path in this case is illustrated in blue in Fig. 13. The pulses for M_g are shown in Fig. 13(b). Then v_s can be ramped from 0 V to nominal voltage and C_{aP} and C_{aN} remain charged near $2V_s$; the main self-powered mechanism can then take over. The voltage-balancing snubber is just approximated by C_{aP} and C_{aN}, and their respective blocking diodes, because it is assumed that the currents involved are relatively small. The excess-power circuit components D_{zgd1}, D_{zgd2}, R_{ex}, and Q_{ex} are approximated as the variable resistance R_x.

VI. Circuit Simulation Results

The setup provided in Fig. 3 was used in the simulations with a V_S = 1.2 kV and a current source load of 10 A. The following two sections present the operation of the two proposed circuits.

A. Voltage Balancing Circuit

The parameters of the simulated switching position are shown in Table II. The voltage balancing action of the circuit was simulated using OrCAD® PSpice®. Simulations were done utilizing Wolfspeed® SiC MOSFET PSpice® models with the turn-ON of $S2$ modeled with a ramp function. The calculated and simulated values for $v_{C_b}/10$ and v_{C_g} during the turn-on compensation event with 2.4 kV across $S1$ and $S2$ and 10 A of resistive load are shown in Fig. 14. The comparison between the two is not without some difference, but this does indicate a good starting point for choosing the parameter values of the circuit. In Fig. 15, the calculated and simulated values for $v_{C_b}/10$ and v_{C_g} during the turn-on compensation event with 2.4 kV across $S1$ and $S2$ and 10 A of current-source load are shown.

In this case, the equilibrium value for the calculations from Section III.B step 3 was chosen based on the MOSFET PSpice® model. The circuit shown in Fig. 6 can be used for this purpose.

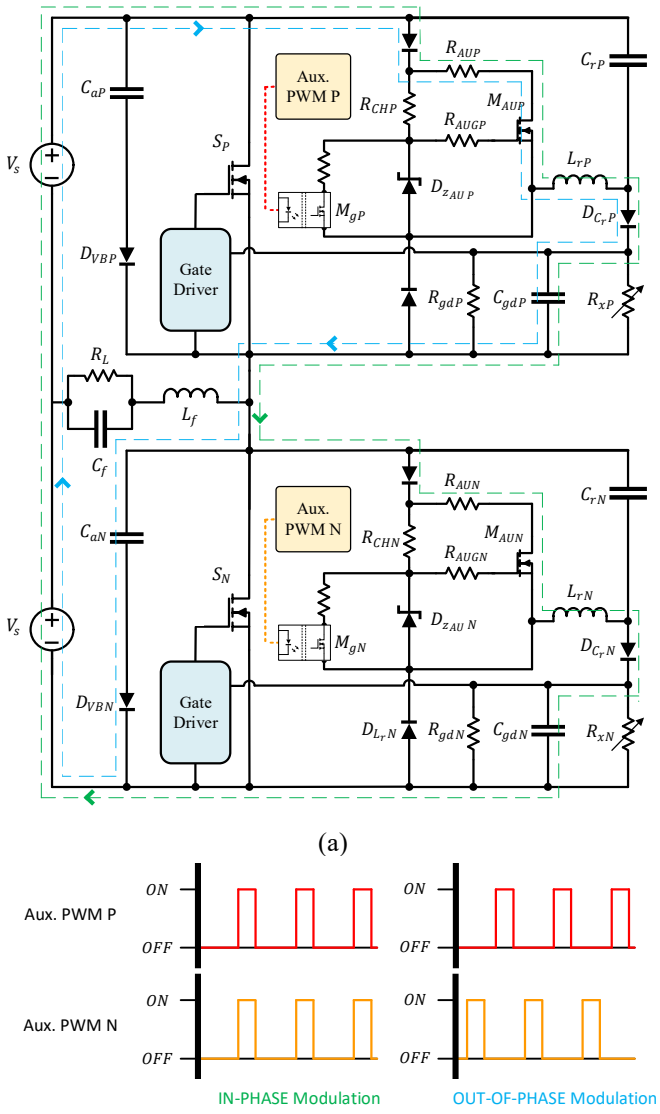

Fig. 13. (a) Start-up currents with in-phase and out-of-phase bucking pulses. (b) The in-phase and out-of-phase modulation pulses.

By injecting the load current into the compensation network, the model will naturally come to the steady-state value. Here, a non-conservative value of C_b was chosen. The peak shown in the calculated values of $v_{C_b}/10$ comes from assuming two different values for $i_1(t)$ ($\mathcal{L}^{-1}\{I_1(s)\}$) in Section III.B.

During MODE I the value of $i_1(t)$ ramps from 0 A at a rate determined the rise time of the MOSFET (i.e., 333 A/µs). Once $t_{V_g=V_{g,on}}$ a steady state value of $i_1(t)$ = 5.0 A is used. This is a large percentage of the load current for this particular design, however, this equilibrium value is highly dependent upon the values of $R_{g,off}$ and V_g^- and can be significantly reduced. For example, the use of $R_{g,off}$ = 5 Ω and V_g^- = -3 V would require a MODE II value of $i_1(t)$ = 1.9 A. Also worth noting is that the $i_1(t)$ does not increase linearly with the load current, so a factor of 2 increase of I_L does not require a factor of 2 increase of $i_1(t)$ as described by the defining equation for MOSFET current in

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TABLE II
CIRCUIT PARAMETERS

Parameter	Value	Rating
C_a	33 nF	2 kV, 19 mΩ
C_b	0.33 nF	1 kV,
R_{gg}	10 Ω	0.5 W
C_{gd}	10 µF	35 V
V_g^-	-5 V	n/a
$R_{g,on}$	5 Ω	0.25 W
L_r	10 mH	0.5 A
C_r	0.220 nF	2 kV
$S1, S2$	C2M0045170D	1.7 kV, 72 A
M_{AU}	SCT2750NYTB	1.7 kV, 6 A
V_g^+	20 V	n/a
$R_{g,off}$	2.5 Ω	0.5 W
$D_{L_r}, D_{C_r}, D_{C_b}, D_{gg}$	CD214A-R12000	2 kV, 2 A

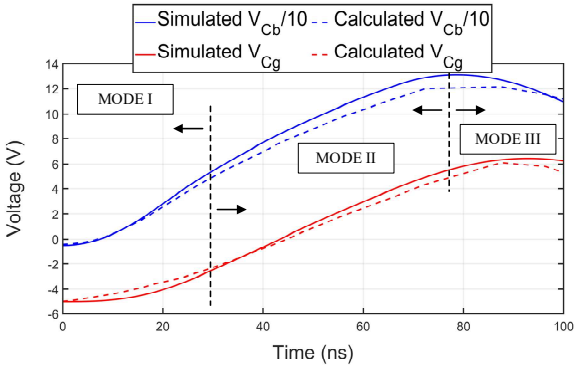

Fig. 14. Calculated vs simulation values of V_{Cb}/10 and V_g for a resistive load.

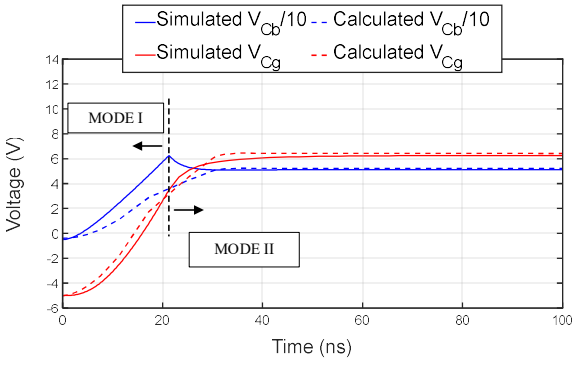

Fig. 15. Calculated vs simulation values of V_{C_b}/10 and V_g for a current-source load.

the saturation region.

It should be noted that the gate voltages during these transients is above the threshold, but much lower than typical ON-state drive voltages. This would result in operation of the MOSFET in the saturation region for a small time. Operating in the saturation conduction region will induce higher switching losses in the switched that is being forced ON by the voltage-balancing circuit which in the case of Fig. 16 and Fig. 17 is $S1$. However, this voltage-balancing scenario should not occur at every switching cycle. This example is also demonstrating a worst-case scenario. With this circuit, care should still be taken to match the ON and OFF behavior of all MOSFETs that are series-connected. The simple voltage rise delay associated with the charging of C_b is enough to guarantee a safe operating voltage when t_{off} is relatively small (< 10 ns).

B. Self-Powered Circuit

Simulations of the novel self-powered circuitry from Fig. 10 were performed with a setup as shown in Fig. 3. The switching frequency for $S1$ and $S2$ were chosen as 10 kHz. In Fig. 18, $v_{C_{gd}}$, and the current through L_r, i_{L_r}, are shown during the 10 kHz operation. The bucking mode start-up i_{L_r} waveforms is nearly identical in shape to that in Fig. 18 but may differ in magnitude and frequency.

VII. CIRCUIT EXPERIMENTAL RESULTS

The tested 3.3-kV switching position formed by the series connection of two 1.7 kV SiC MOSFETs is presented in Fig. 19. Though each switch would theoretically be a separate installation with its own fiber optic signaling, this switching position was designed to operate using a single gate signal for simplicity. A high-side driver was used to gate the top switch

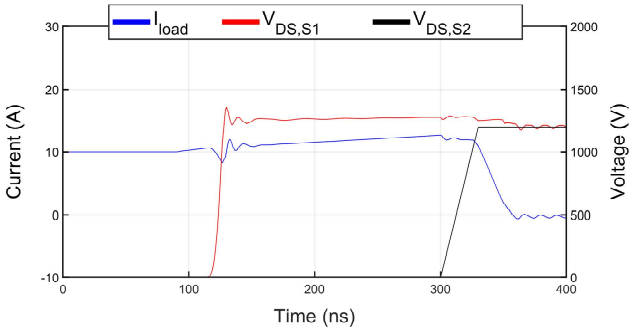

Fig. 16. Simulation results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-OFF with a 200 ns delay in offset time with a current-source load.

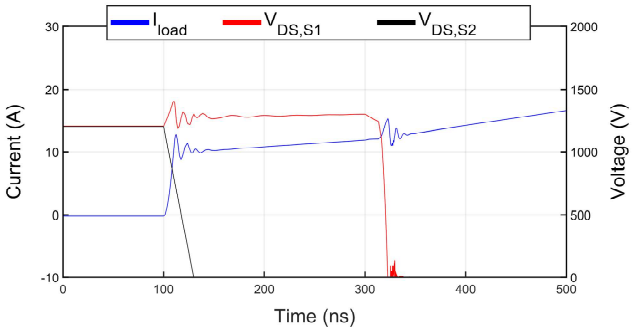

Fig. 17. Simulation results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-ON with a 200 ns delay in offset time with a current-source load.

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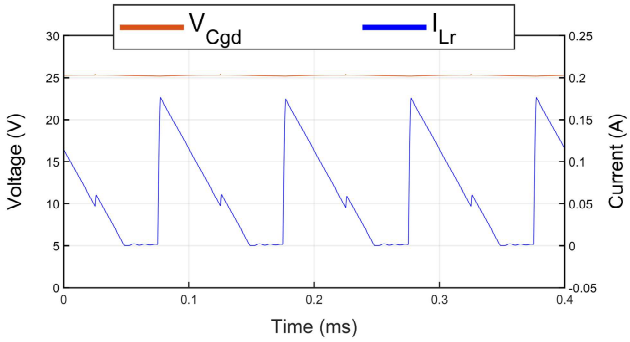

Fig. 18. I_{L_r}, and V_{Cgd} during turn ON and turn OFF of $S2$.

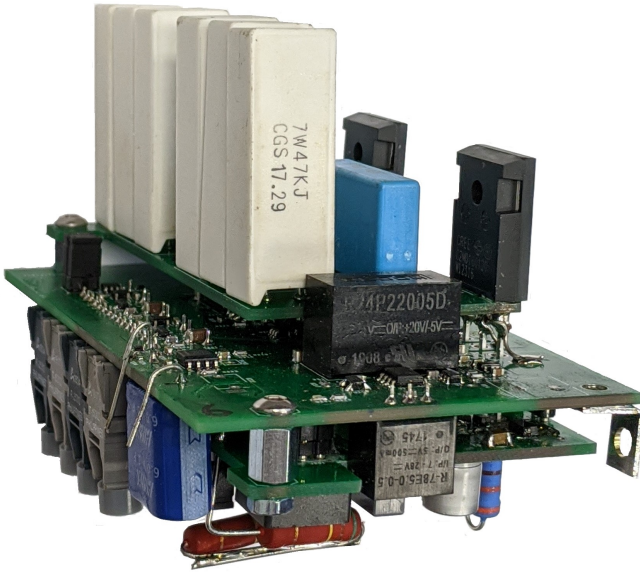

Fig. 19. Photograph of 3.3 kV switching position prototype.

using the same signals as the low-side circuit.

This configuration is a good representation of another possible trade-off for this type of module switching position. It may be more cost effective to pre-package series devices up to the limits for conventional high-side ICs and then stack these higher-voltage units together. However, this does reintroduce common-mode current within the shared PCBs.

A. Voltage-Balancing Circuit

The testing configuration is shown in Fig. 3 with V_S = 1.2 kV. The clamped inductive load current is 10 A. Like the simulation results in Fig. 14, Fig. 20 shows experimental waveforms for the $v_{C_b}/10$ and v_{C_g} for $S2$ when it is delayed relative to $S1$ by around 200 ns as well as the full turn-ON transient. This delay emulates either a false turn-ON signal on one of the devices or a large difference in dv/dt values between series-connected devices. At t = 0 s, $S1$ begins to turn ON. The voltage across C_b rises until v_{C_g} increases to the point where $S2$ begins to take significant current and then both stay around a constant voltage

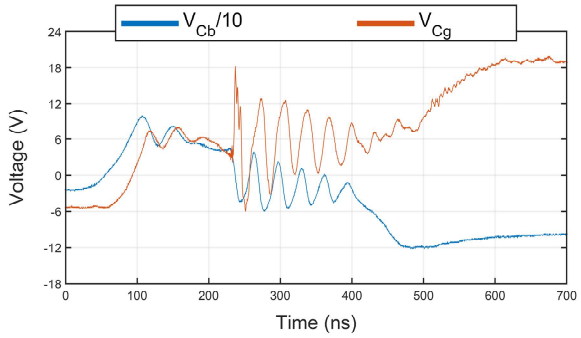

Fig. 20. Experimental results of $V_{Cb}/10$ and V_g with $S2$ delayed by 220ns.

until the gate driver for $S2$ takes over at t = 220 ns; at which point, v_{C_g} starts to rise to the nominal ON-state gate voltage of 20 V. The starting voltage of C_b differs from the V_g^- predicted by the simulations due to the reverse-recovery charge of D_{C_b} within the voltage-balancing circuit. This allows C_b to be charged by C_a during a short time. The recovery charge of D_{gg} also contributes to some of the ringing observed in v_{C_g} at t = 220 ns. These affects could be minimized with the use of low reverse recovery diodes and low-inductance components and layout.

The voltage across $S1$, $v_{DS_{S1}}$, and $v_{DS_{S2}}$ are shown in Fig. 21 along with the load current through the switching position for various values of t_{off} during the turn-OFF transient. There is an initial overvoltage event in $v_{DS_{S2}}$ above 1.2 kV followed by a convergence onto 1.2 kV, which is the voltage of C_a. As discussed in Section III and demonstrated in Section IV a small percentage of the load current is diverted from $S2$ to the voltage balancing circuit. This small diverted current keeps C_g charged to a steady-state value during the transient and forces $S2$ into the saturation conduction region for a short period of time rather than experiencing a catastrophic overvoltage.

The turn-ON transient is illustrated in Fig. 22. These voltages were measured with TPP0850 probe from Tektronix® utilizing tip-to-BNC adapters and the voltage was stepped down using techniques suggested in [35] for an approximate bandwidth of 300 MHz. A 1.6 kV spike in $v_{DS_{S2}}$ from Fig. 21 comes from a slight under-sizing of C_a and C_b and inductance in the compensation and measurement paths. This is known because the voltage across C_b in Fig. 20 should account for the majority of the voltage overshoot across $S2$.

B. Self-Powered Circuit

The waveforms for i_{L_r} and $v_{C_{gd}}$ during the bucking operation of the start-up circuit are shown in Fig. 23. These waveforms were taken at nominal bus voltage (i.e., 2.4 kV). The operating duty cycle at lower voltages would be larger and thus the positive slope section of the waveforms would be longer. A noticeable ripple in $v_{C_{gd}}$ can be seen. This can obviously be reduced by increasing C_{gd}, but this amount of ripple is acceptable for this application because C_{gd} is buffered by a variable input voltage power supply ICs. For these waveforms,

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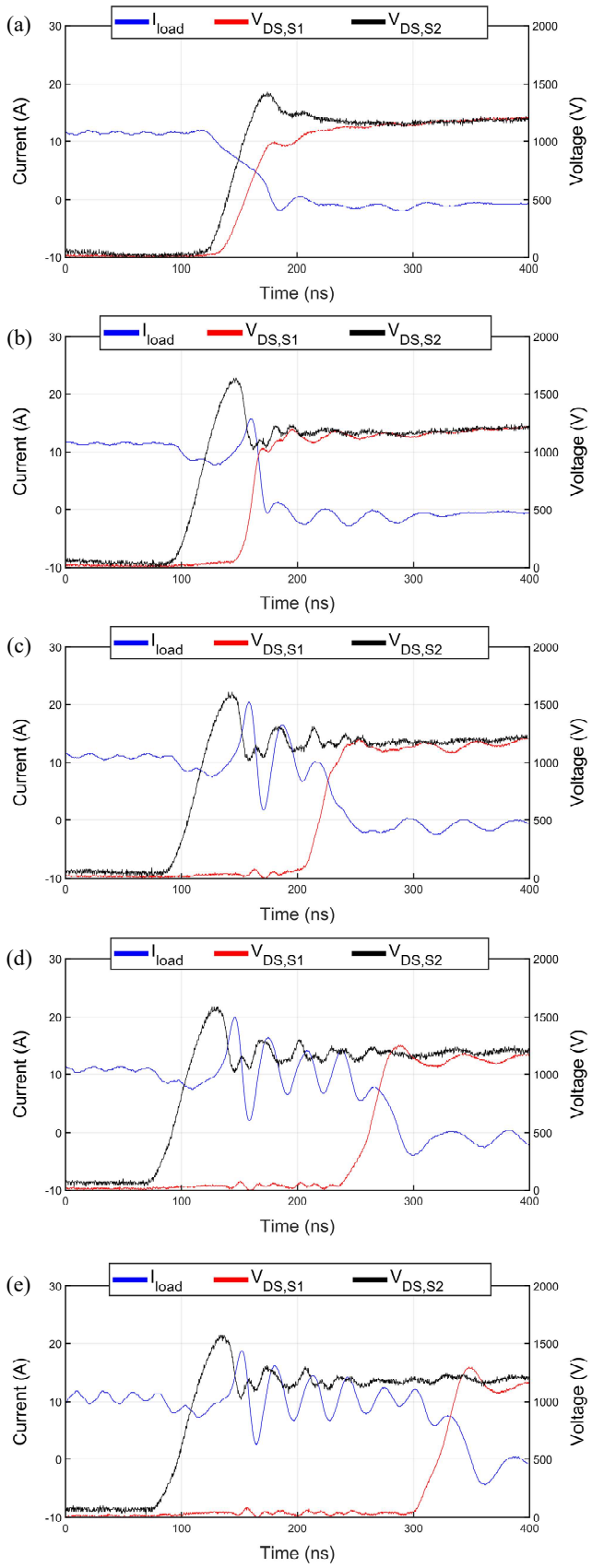

Fig. 21. Experimental results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-OFF for (a) 10 ns (b) 50 ns (c) 100 ns (d) 150 ns (e) 200 ns offset time.

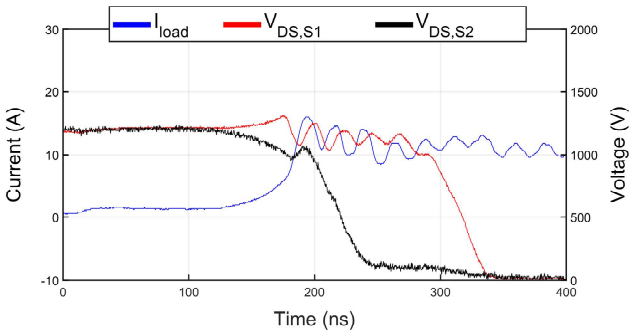

Fig. 22. Experimental results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-ON with a 200 ns delay in offset time.

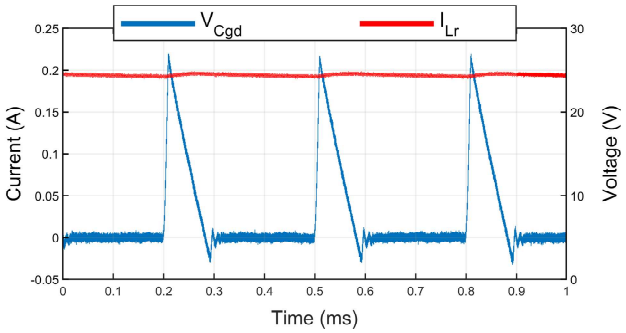

Fig. 23. Experimental waveforms of I_{L_r} and $V_{C_{gd}}$ during bucking start-up operation.

the switching frequency of the bucking, and thus M_{AU}, is 3 kHz. During normal operation, this same waveform shape is seen in L_r when C_r resonates into L_r and M_{AU} is OFF; however, the peak and frequency of i_{L_r} may change depending on the operating frequency of $S1$ and $S2$ as was the case in Fig. 18. For the tested prototype a switching frequency of 3 kHz was chosen to reduce the thermal management requirements of M_{AU}.

It is important to choose a value of L_r and a switching frequency that results in a discontinuous conduction mode for the inductor. This ensures that M_{AU} operates with quasi-ZCS at turn-ON and reduces the required thermal management. Also, this avoids the problem with diode reverse recovery of D_{C_r} affecting the energy transfer from C_r to L_r. The effect of the reverse recovery can be seen in Fig. 24 where L_r is operating in a semi-continuous conduction mode. The reverse recovery charge depleted C_r and this results in a lower energy transfer to L_r. This can be seen in the relative peaks of the current at t ≈ 0.0 ms and t ≈ 0.1 ms. Because the discharging current slope of L_r is a function of its inductance and $V_{C_{gd}}^*$, this sets the upper limit of the buck converter switching frequency.

C. Start-Up for a Half-Bridge Application

The half-bridge test circuit is shown in Fig. 25. The top and bottom devices of the half-bridge circuit are formed using two stackable switching positions. The performance of the half-bridge start-up procedure explained in Section V appears

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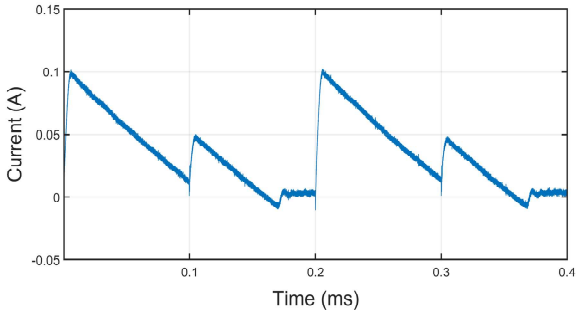

Fig. 24. Experimental waveforms of I_{L_r} where L_r operating in continuous conduction mode.

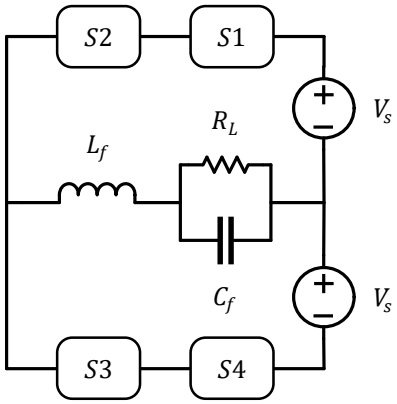

Fig. 25. Half-bridge testing configuration.

in Fig. 26 and Fig. 27 where waveforms for v_{C_a1} and v_{C_a2} and i_{L_r} are shown. The in-phase bucking modulation results in a constant C_a equal to V_s. The out-of-phase bucking modulation results in a C_a much closer to the desired value of $2V_s$. A voltage ripple in v_{C_a} can be seen in Fig. 27. This is due to the discharging of C_a through R_b. To reduce the voltage ripple across C_a, a larger value of R_b can be used or the switching frequency of M_{AU} can be increased.

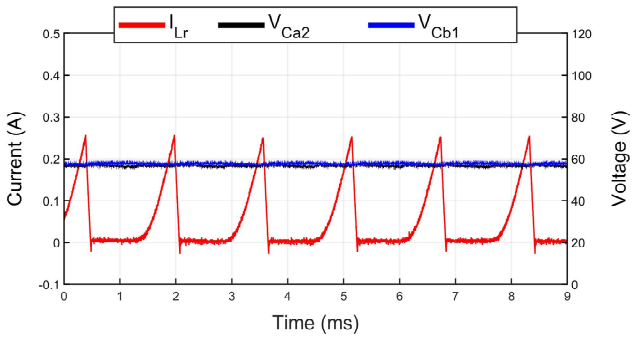

Fig. 26. Voltage-balancing circuit capacitor voltage and self-power inductor current with in-phase start-up modulation.

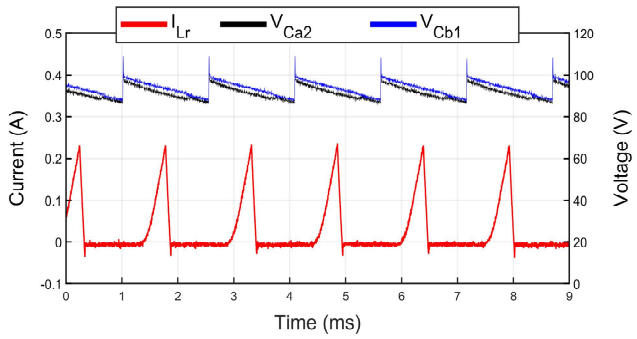

Fig. 27. Voltage-balancing circuit capacitor voltage and self-power inductor current with out-of-phase start-up modulation.

VIII. Protection Concerns

It is important that the switching position reacts appropriately if the switching position is operating incorrectly or is experiencing an undesired condition. For this reason the switching position was designed with the following protection capabilities:

1) Desaturation - An overcurrent condition turns the power semiconductor S OFF and generates a TTL error flag.

2) Gate Driver Undervoltage – The switching position will detect a malfunction of the gate drive power supply IC or a low voltage across C_{gd}, generating an error flag.

3) Device Overvoltage - A resistor divider and voltage comparator are used to monitor the voltage across the power semiconductor device to detect a static voltage imbalance. If the voltage is too high, then this implies the voltage is no longer being properly shared by series con nected switching positions.

4) PWM Interlocks – Open-collector logic is used with the auxiliary and main PWM to ensure that neither are ON at the same time. This prevents spurious tripping and damage to the start-up circuit if these signals are malfunctioning.

5) Auxiliary PWM Ride-Through – In the event that the converter in which this switching position is used requires an emergency shut-down, the switching position must be able to survive for a short time without any possibility to power itself. This is due to the normally-ON configuration of the start-up circuit. To provide this ride-through capability, the power rail for the auxiliary PWM fiber optic receiver circuit has been isolated through a diode from the main power rail for the gate drive and diagnostic circuitry. On this isolated power rail, a large reservoir of energy is placed. For the switching position in this paper a 1.5 F supercapacitor is used. This means, if power on the board is lost then the supercapacitor can drive M_g without having to provide power to the rest of the circuits. This energy reservoir can then be sized based on the drive current for M_g and amount of time required to discharge the energy storage in the converter.

The error signals from the desaturation, gate-driver undervoltage, and device overvoltage are all combined with TTL logic gates and then trigger an active-low master fault flag. This single flag is sent by fiber optic back to the controller. This

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is important because if one of the series connected switching positions has a fault the controller needs to quickly shut-down the converter.

IX. Conclusions

A novel self-powered modular switching position with voltage-balancing ability for series-connected MOSFETs was presented. A new step-by-step procedure for choosing the components for the new configuration of the voltage-balancing circuit as well as the equations defining the self-powered behavior were also given. In addition, a novel start-up scheme for the self-powering circuitry was introduced. Lastly, the protection circuitry needed for the switching position is presented.

The behavior of the circuitry was confirmed by simulations. The voltage-balancing behavior of a 3.3-kV switching position made up of two 1.7-kV SiC MOSFETs was experimentally verified under current-source loading demonstrating the feasibility of the proposed ideas. In particular, the prototype was also experimentally shown to be capable of powering itself from the voltage across it.

Appendix

Below is an example design of the voltage-balancing circuit for the circuit in Fig. 3 with a current-source load:

1) Decide on the gate driver parameters. They are chosen to be

$$R_g = 2.5\ \Omega\,,$$
$$V_g^+ = 20\ \text{V}\,,$$
$$V_g^- = -5\ \text{V}\,.$$

2) Choose the maximum voltage overshoot, ΔV_{DS}, for the switch S. The value is chosen to be

$$\Delta V_{DS} = 200\ \text{V}\,.$$

Then, R_{gg} is calculated as

$$R_{gg} < \frac{(200\ \text{V})(2.5\ \Omega)}{(3\ \text{V}) - (-5\ \text{V})},$$
$$R_{gg} < 30\ \Omega\,,$$

with $V_{g,on} \approx 3$ V. An R_{gg} of 10 Ω is chosen.

3) Determine the current balance between i_1 and $i_{\text{R}_{S2}}$ during MODE II. The circuit parameters are

$$I_L = 10\ \text{A}\,,$$
$$V_s = 1200\ \text{V}\,.$$

The steady-state values of V_{C_g} and V_{C_b} from the model simulations are

$$V_{C_g,ss} = 6.5\ \text{V}\,,$$
$$V_{C_b,ss} = 50\ \text{V}\,.$$

The value of i_1 and $i_{\text{R}_{S2}}$ are the given by

$$i_1 = \frac{6.5\ \text{V} - (-5\ \text{V})}{2.5\ \Omega},$$
$$i_1 \approx 5\ \text{A}\,,$$
$$i_{\text{R}_{S2}} = 10\ \text{A} - 5\ \text{A} = 5\ \text{A}\,.$$

4) Determine the value of C_b. The worst-case gate pulse offset is chosen as

$$t_{off} = 200\ \text{ns}\,.$$

The calculated waveforms for v_{C_g} and $v_{C_b}/10$ for different values of C_b is shown in Fig. 28.

When C_b is 100 nF, v_{C_g} takes almost the entire t_{off} to charge to $V_{g,on}$. This indicates an oversizing of C_b. At 0.33 nF, v_{C_b} charges above $V_{C_b,ss}$ before $v_{C_g} = V_{g,on}$. This indicates an appropriate value of C_b. From this analysis the chosen capacitor values are

$$C_b = 0.33\ \text{nF}\,,$$
$$C_a = 100C_b = 33\ \text{nF}\,.$$

5) Calculate the extra energy absorbed by C_a. From gate drive components datasheets, a mismatch in propagation delay can be predicted between any two devices connected in series. An average value of t_{off} = 20 ns is assumed. From the calculated waveforms, the RMS current into C_a is 2.9 A. The average energy absorbed by C_a is then

$$\Delta E_{C_{a,avg}} = (1200\ \text{V})(2.9\ \text{A})(20\ \text{ns}) = 70\ \mu\text{J}\,.$$

The power required to be dissipated by R_b is

$$P_{C_a} = (70\ \mu\text{J})(10\ \text{kHz}) = 0.8\ \text{W}\,.$$

The value of R_b can the be chosen as

$$R_b < \frac{(1200\ \text{V})^2}{0.8\ \text{W}}(0.5)$$
$$R_b < 900\ \text{k}\Omega$$

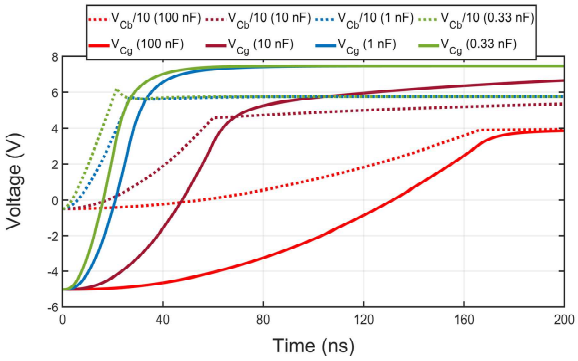

Fig. 28. V_{C_g} and $V_{C_b}/10$ for different values of C_b.

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by assuming d_{avg} = 0.5.

Assuming a mismatch in OFF-state leakage current of 12 μA between the power devices R_a can be determined by

$$R_a = \frac{1200\ \text{V}}{10(12\ \mu\text{A})}$$

$$R_b = 10\ \text{M}\Omega$$

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