

A 150-kW 99% Efficient All Silicon Carbide Triple-Active-Bridge Converter for Solar-Plus-Storage Systems

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Abstract—Solar-plus-storage systems could effectively mitigate uncertainties of the photovoltaic (PV) generation and improve system reliability by adding an integrated battery energy storage system. As a three-port bidirectional isolated dc-dc converter with soft-switching capability, the triple-active-bridge (TAB) converter inherently match the requirements of the solar-plus-storage system. However, challenges still remain in the TAB converter design to further improve the system efficiency. In this paper, the detailed design, implementation, and demonstration for a silicon carbide (SiC) 150-kW TAB converter are presented. Starting from a brief review of the TAB converter, the modulation scheme, power characteristics, and soft-switching region are analyzed. Then, the detailed design of the H-bridge converter building block is given. To improve the system efficiency, a comprehensive characterization of the SiC gate driver with various external gate resistances is performed to address tradeoffs between switching loss and voltage overshoot during transients, as well as the thermal performance of the H-bridge building block. In addition, the design and characterization for the 20-kHz three-port transformer are also given. Comprehensive experimental studies are conducted on a full-power prototype to verify the proposed design. With a measured 99.1% peak efficiency, the proposed TAB converter can fulfill the requirements for solar-plus-storage applications.

Index Terms—Solar-plus-storage systems, triple-active-bridge converter, high efficiency, thermal modeling, transformer design.

I. INTRODUCTION

Compared with the conventional line-frequency transformers, a solid-state transformer (SST) utilizes active power switches and medium- or high-frequency (HF)

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transformer to achieve the power transfer and voltage isolation [1]. Due to the use of high switching frequencies in an SST, the volume and weight of passive components can be significantly reduced, and thus, the system power density can be notably increased. Moreover, the SST also enables new features that the conventional power transformer does not possess. For instance, the use of the active power semiconductor devices brings the possibilities of active power control and fault tolerant capabilities, which can improve the system efficiency and robustness [1], [2]. In addition, an SST can achieve the power conversion between dc power ports, while the conventional line-frequency transformer can only operate in an ac power grid. Thus, SST could perfectly fulfill the needs for grid integration of the distributed energy resources (DERs) [3].

With the same power capacity, although the hardware cost of the SST is still higher than the conventional line-frequency transformer, the soft cost, which includes the cost for install labor and equipment, logistics, land acquisition, maintenance and etc., of SST can be much lower due to its high power density. For example, based on the U.S. Department of Energy standard [37], the required efficiency for a 150 kVA low-voltage dry-type line-frequency three-phase transformer is 98.83%, and a well-designed SST could also achieve a similar performance [1]. In contrast, considering the power density of the transformer, the same power rating and efficiency level SST would occupy much less space compared with the conventional transformer, as the volume and weight of a typical pad mount 150 kVA three-phase line-frequency transformer can be about 4.2 m³ and more than 3000 lbs. [1].

In addition, with the development of the DERs, additional equipment like static synchronous compensator (STATCOM) may be necessary to stabilize the power grid and improve power quality as the conventional line-frequency transformer cannot actively control the active and reactive power. As the SST could achieve the active power control as well as reactive power compensation without additional STATCOM, the cost difference between an SST-based distribution system and a conventional line-frequency transformer based distribution system will be further narrowed [1].

The solar-plus-storage system is a typical configuration for a DER generation system, where a battery energy storage system (BESS) could be integrated with a photovoltaic (PV) system to mitigate the uncertainties of the PV system and improve the system reliability [4]. In a dc-coupled solar-plus-storage system, both the PV systems and BESS are connected to the common dc bus and provide the energy to the grid-tied inverter or directly to the dc microgrid. A bidirectional multi-port dc-dc converter is desired to achieve the power transmission among the PV arrays, BESS, and the common dc bus. Among various SST topologies, the triple-active-bridge (TAB) converter, where three dc-ac converters are coupled through a three-port transformer, can enable galvanic isolation and transfer power among three dc ports with less number of components [5]-[8]. Moreover, similar to its two-port counterpart, i.e., the dual-active-bridge (DAB) converter [9], [10], [26], the TAB converter can operate at the zero-voltage-switching (ZVS) mode to reduce the switching loss. Thus, the TAB converter inherently satisfies the needs of the solar-plus-energy system.

In the conventional dc-coupled solar-plus-storage system, the BESS and PV are connected to a common dc bus through the use of dc-dc converters, as the output voltages of PV and BESS could be different. Compared with the conventional system configuration, the TAB converter based solar-plus-energy configuration enables the integration at the converter level, which will provide a faster dynamic response and improve the system robustness, as a centralized controller could adjust the power distribution between PV port and BESS port rather than controlling power through communication between different dc-dc converters [5], [31], [32]. However, the design of a high-power high-efficiency TAB converter still remains challenging. Although the TAB converter can almost eliminate the turn-on loss when it works in the ZVS region, the turn-off loss remains and can reduce system efficiency, especially when a higher switching frequency is desired to reduce the system volume. Moreover, the significant turn-off loss can lead to the junction temperature rise, which further reduces the system efficiency, and may even result in device failures.

The development of wide bandgap (WBG) devices, especially silicon carbide (SiC) MOSFETs, enables new possibilities for the TAB converter. Compared with their Si counterparts, the fast switching speed and low switching loss of SiC devices allow for higher switching frequency. Moreover, with similar power rating, the footprint of the SiC power module is much smaller than the Si modules. Thus, the converter power density can be significantly improved [1]. In addition, the high temperature operating capability of SiC devices can also increase the converter system reliability. Even though, the optimized design of a SiC-based TAB converter is still necessary to achieve high efficiency. The high switching speed enabled by SiC devices, especially the high di/dt , during the switching transient can lead to severe voltage oscillation and overshoot. The high voltage overshoot may also cause the device failure [11]. Furthermore, the transient voltage overshoot can be even larger if a low external gate resistance is adopted in the gate driver to further reduce the switching loss [12], [13]. Thus, a holistic design and optimization approach for

the SiC-based TAB converter is necessary to maximize the system efficiency, including the evaluation and selection of the external gate resistance, the design of the power electronic building block (PEBB), and design of the high-frequency (HF) three-port transformer.

In the existing literature, the modeling and basic power control schemes of the TAB converter have been discussed in [5], [7]. However, the detailed analysis of the ZVS operation was not provided. Although the ZVS region has been discussed in [8], the TAB converter used in the paper is a current-source-based TAB converter, which has different characteristics to the commonly used voltage-source-based TAB converter. The ZVS analysis for the voltage-source-based TAB converter has been presented in [14] and [31]. However, the closed-form ZVS condition for the TAB converter was not given. Similarly, [32] and [33] discussed the ZVS operation of the TAB converter, but the closed-form ZVS condition was not given as well. The efficiency improvement of the TAB converter has been discussed in [34], where the focus is to investigate different control schemes to improve the ZVS region of the TAB converter.

In this paper, detailed analysis, design, prototyping, and testing of a 150-kW all-SiC TAB converter is presented to fulfill the high efficiency requirement of the solar-plus-storage systems. First, a review of the TAB converter, including the modulation scheme, power transmission characteristic, and soft-switching analysis, has been given. A closed-form ZVS condition for the TAB converter is given. Then the design of the PEBB has been provided. The gate resistance is carefully evaluated and characterized to address the tradeoff between the system efficiency and transient voltage overshoot. Besides, the heatsink is also characterized to evaluate the PEBB thermal performance. In addition to the optimized design of the PEBB, the design and characterization of the three-port transformer also has been presented. A comprehensive experimental study is performed on the TAB converter prototype, with the results demonstrating the effectiveness of the design. The measured peak efficiency of the TAB converter is 99.1% and the full load efficiency is 98.5%. The major contributions of this paper include:

1. Based on the detailed TAB converter analysis, a closed-form ZVS condition is presented.
2. Comprehensive characterization and optimization for the SiC-based PEBB have been conducted to minimize the switching loss and validate the thermal performance.
3. The detailed design procedure and characterization method for the three-port HF transformer are given considering the high-efficiency target.

The remainder of the paper is organized as follows. Section II reviews the modulation scheme and power transmission characteristic of the TAB converter, and the ZVS operating region also has been analyzed. Section III presents the design of the PEBB, including selection of the gate resistance to trade transient voltage overshoot against the converter efficiency, and the thermal performance characterization. The optimized design of the three-port transformer is given in Section IV, as well as the transformer characterization. Comprehensive

experimental studies have been performed on the TAB converter prototype to validate the effectiveness of the proposed design, and the results are given in Section V. Section VI concludes this paper.

II. A REVIEW OF THE TAB CONVERTER

A. Modulation and Power Transmission Characteristics

Fig. 1(a) shows a typical schematic of a TAB converter, where three H-bridge converters, i.e., H1, H2, and H3, are coupled through a three-port transformer, whose turns ratio is $n_1:n_2:n_3$, Q_1-Q_{12} are the power devices, L_1-L_3 are the winding leakage inductances of the transformer (including externally connected inductances), C is the output capacitor, R_L represents the load, U_{in1} and U_{in2} are two dc power inputs, which can be connected to PV systems and/or BESS in the solar-plus-storage application, V_1 , V_2 , and V_3 are the outputs of those three H-bridge converters respectively, I_{L1} , I_{L2} , and I_{L3} are the current flowing through L_1 , L_2 , and L_3 respectively. The power transmission among three ports inside of the TAB converter can be achieved by adjusting the phase-shift angles of those three H-bridge converters. Fig. 1(b) shows the most straightforward single-phase-shift (SPS) modulation scheme, where the output of each H-bridge converter is fixed as 50% duty ratio, F_s is the switching frequency, $T_s=1/F_s$ is the switching period, ϕ_{12} , ϕ_{13} , and ϕ_{23} represent the phase-shift ratios.

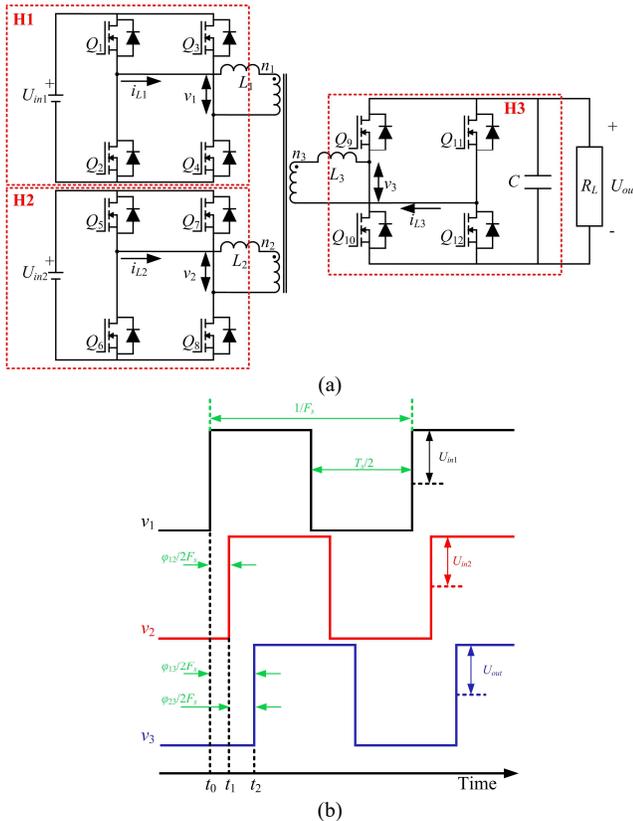


Fig. 1. (a) Schematic of the TAB converter and (b) SPS modulation scheme.

In order to model the power transmission characteristic of the TAB converter, the Δ -equivalent model can be utilized [14], which can also be called as the π -equivalent model [7]. Fig. 2

shows the equivalent model of the TAB converter, where P_1 , P_2 , and P_3 represent the power flowing through each dc port, P_{12} , P_{13} , and P_{23} are the power flowing between two dc ports, L_{12} , L_{13} , and L_{23} are the equivalent leakage inductances of the three-port transformer, which satisfy

$$\begin{cases} L_{12} = \frac{\sum L}{L_3} \\ L_{13} = \frac{\sum L}{L_2} \\ L_{23} = \frac{\sum L}{L_1} \\ \sum L = L_1 L_2 + L_1 L_3 + L_2 L_3 \end{cases} \quad (1)$$

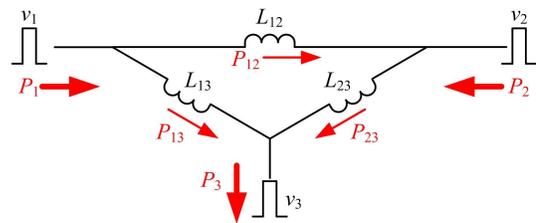


Fig. 2. The Δ -equivalent model of the TAB converter.

The Δ -equivalent model of the TAB decouples the three ports to three two-port pairs, and the power transferred between the i^{th} port and j^{th} port can be written as [7], [14]

$$P_{ij} = \frac{n_i}{n_j} \frac{|v_i| |v_j| \phi_{ij} (1 - \phi_{ij})}{2F_s L_{ij}} \quad (2)$$

In this work, considering the use of a 1500-V PV system, the voltage for maximum power point tracking (MPPT) range from 800 V to 1300 V [15]. Considering the typical BESS voltage for 1500-V PV system could range from 800 V to 1300 V depending on the battery configuration [28], [29]. The battery voltage is set from 800 V to 1300 V in this design, which means the battery port voltage rating is the same as the PV port. The output voltage of the TAB converter is set as 1300 V. The maximum output power of the TAB converter is set to be 150 kW with each input port providing 75 kW. The switching frequency of the converter is 20 kHz.

Based on (2), the leakage inductances are designed as $L_1=19 \mu\text{H}$, $L_2=19 \mu\text{H}$, and $L_3=31 \mu\text{H}$, which are calculated by supposing $P_{12}=P_{13}=P_{23}=80 \text{ kW}$, and thus, the required 75 kW power transferring requirement could be achieved. In the inductance calculation, the input voltages are set as $U_{in1}=U_{in2}=800 \text{ V}$ and the output voltage is set as $U_{out}=1300 \text{ V}$. The phase-shift ratio ϕ_{ij} is set as 0.5, as the maximum power will be obtained when $\phi_{ij}=0.5$ [9]. The maximum power that PV and battery could deliver to the output port is 150 kW. The transformer turns ratio is designed as $n_1:n_2:n_3=1:1:1$. At the full output power condition, the root-mean-square (RMS) value of three leakage inductor currents are $I_{L1}=67.5 \text{ A}$, $I_{L2}=67.5 \text{ A}$, and $I_{L3}=135 \text{ A}$, respectively. Table I summaries the TAB converter parameters.

TABLE I. TAB CONVERTER PARAMETERS

Parameter	Value
PV side input voltage U_{in1}	800-1300 V
Output voltage U_{out}	1300 V
Leakage inductance L_1	19 μ H
Leakage inductance L_3	31 μ H
PV side maximum input power P_1	75 kW
Maximum output power P_3	150 kW
Battery side input voltage U_{in2}	800-1300 V
Switching Frequency	20 kHz
Leakage inductance L_2	19 μ H
Turns ratio $n_1:n_2:n_3$	1:1:1
Battery side maximum input power P_2	75 kW

B. Soft-Switching Analysis

Similar to a two-port DAB converter, the TAB converter can operate at the ZVS mode to reduce the switching loss. Thus, the converter switching frequency can be increased to reduce the volume of passive components and improve the power density. Moreover, the ZVS region could be enlarged by adopting advanced phase-shift schemes [9], [10], [16], or implementing adaptive inductor [20]. In this paper, the ZVS region analysis is performed based on the adopted SPS modulation scheme.

As Fig. 1(b) shows, the output voltage of the H-bridge converter in the first half period is symmetric to the second half period due to the fixed 50% duty ratio. Thus, the first half period will be only analyzed. Assuming that the H-bridge converter H1 starts to generate $V_1=U_{in1}$ at time instant t_0 , i.e., switches Q_1 and Q_4 turn on at t_0 . Similarly, converters H2 and H3 begin to generate the positive output at $t_1=\varphi_{12}/2F_s$ and $t_3=\varphi_{13}/2F_s$, respectively. Ignoring the output capacitances of the power switches, converter H1 can achieve the ZVS at t_0 if $I_{L1}(t_0) < 0$. In other words, before Q_1 and Q_4 turning on, the current I_{L1} flows through the antiparallel diodes of Q_1 and Q_4 if $I_{L1}(t_0) < 0$, and thus, the switches Q_1 and Q_4 can turn on under the ZVS condition. Similarly, the ZVS conditions for converters H2 and H3 are $I_{L2}(t_1) < 0$ and $I_{L3}(t_2) > 0$, respectively. The ZVS condition for the TAB converter can be summarized as follows:

$$\begin{cases} \text{H1 ZVS: } i_{L1}(t_0) < 0 \\ \text{H2 ZVS: } i_{L2}(t_1) < 0 \\ \text{H3 ZVS: } i_{L3}(t_2) > 0 \end{cases} \quad (3)$$

For a TAB converter, the inductor currents satisfy

$$\begin{cases} v_1 - n_1 v_x = L_1 \frac{di_{L1}}{dt} \\ v_2 - n_2 v_x = L_2 \frac{di_{L2}}{dt} \\ n_3 v_x - v_3 = L_3 \frac{di_{L3}}{dt} \\ n_1 i_{L1} + n_2 i_{L2} = n_3 i_{L3} \end{cases} \quad (4)$$

where v_x is the voltage applied to the magnetizing inductance per turn. As $n_1 i_{L1} + n_2 i_{L2} = n_3 i_{L3}$, the inductor current

derivatives also satisfy $n_1 \frac{di_{L1}}{dt} + n_2 \frac{di_{L2}}{dt} = n_3 \frac{di_{L3}}{dt}$. Then the voltage V_x could be calculated based on (4) as

$$v_x = \frac{L_1 L_2 n_3 v_3 + L_1 L_3 n_2 v_2 + L_2 L_3 n_1 v_1}{L_1 L_2 n_3^2 + L_1 L_3 n_2^2 + L_2 L_3 n_1^2}. \quad (5)$$

Based on the SPS modulation scheme shown in Fig. 1(b), the output voltage of converters H1, H2, and H3 can be written as

$$\begin{aligned} v_1 &= +U_{in1} & (t_0 < t < T_s/2) \\ v_2 &= \begin{cases} -U_{in2} & (t_0 < t < t_1) \\ +U_{in2} & (t_1 < t < T_s/2) \end{cases} \\ v_3 &= \begin{cases} -U_{out} & (t_0 < t < t_2) \\ +U_{out} & (t_2 < t < T_s/2) \end{cases} \end{aligned} \quad (6)$$

Without loss of generality, the phase-shift ratios are supposed $\varphi_{12} < \varphi_{13}$. For the situation that $\varphi_{12} > \varphi_{13}$, the analysis will be similar. Combining (4)-(6), the inductor current I_{L1} at time t_0 can be derived as

$$\begin{aligned} i_{L1}(t_0) &= - \left[\frac{2L_3 n_2 n_1 U_{in2} \varphi_{12}}{L_1 L_2 n_3^2 + L_1 L_3 n_2^2 + L_2 L_3 n_1^2} \right. \\ &+ \frac{2L_2 n_3 n_1 U_{out} \varphi_{13}}{L_1 L_2 n_3^2 + L_1 L_3 n_2^2 + L_2 L_3 n_1^2} \\ &+ \frac{L_2 n_3 (n_3 U_{in1} - n_1 U_{out})}{L_1 L_2 n_3^2 + L_1 L_3 n_2^2 + L_2 L_3 n_1^2} \\ &\left. + \frac{L_3 n_2 (n_2 U_{in1} - n_1 U_{in2})}{L_1 L_2 n_3^2 + L_1 L_3 n_2^2 + L_2 L_3 n_1^2} \right] \frac{T_s}{4} \end{aligned} \quad (7)$$

Thus, the ZVS condition for the converter H1 is

$$\begin{aligned} L_3 n_2 [n_2 U_{in1} - n_1 (1 - 2\varphi_{12}) U_{in2}] \\ + L_2 n_3 [n_3 U_{in1} - n_1 (1 - 2\varphi_{13}) U_{out}] > 0 \end{aligned} \quad (8)$$

Similarly, the ZVS conditions for converters H2 and H3 can be derived and the results are given in (9) and (10), respectively.

$$\begin{aligned} L_3 n_1 [(1 - 2\varphi_{12}) n_2 U_{in1} - n_1 U_{in2}] \\ + L_1 n_3 [(2\varphi_{12} - 2\varphi_{13} + 1) n_2 U_{out} - n_3 U_{in2}] < 0 \end{aligned} \quad (9)$$

$$\begin{aligned} L_2 n_1 [(1 - 2\varphi_{13}) n_3 U_{in1} - n_1 U_{out}] \\ + L_1 n_2 [(2\varphi_{13} - 2\varphi_{12} + 1) n_3 U_{in2} - n_2 U_{out}] < 0 \end{aligned} \quad (10)$$

Based on the ZVS conditions given in (8)-(10), Fig. 3 shows the ZVS region of the TAB converter with the proposed circuit parameters considering the PV port voltage varying, supposing $U_{in2}=U_{out}=1300$ V. It can be seen that at least two H-bridge converters can operate at the ZVS mode at any operating point. Especially, the TAB converter can achieve the ZVS in the full operation region when the PV port input voltage $U_{in1}=1300$ V. As mentioned previously, advanced phase-shift scheme can further enlarge the ZVS region, at the cost of control complexity [9], [10], [16].

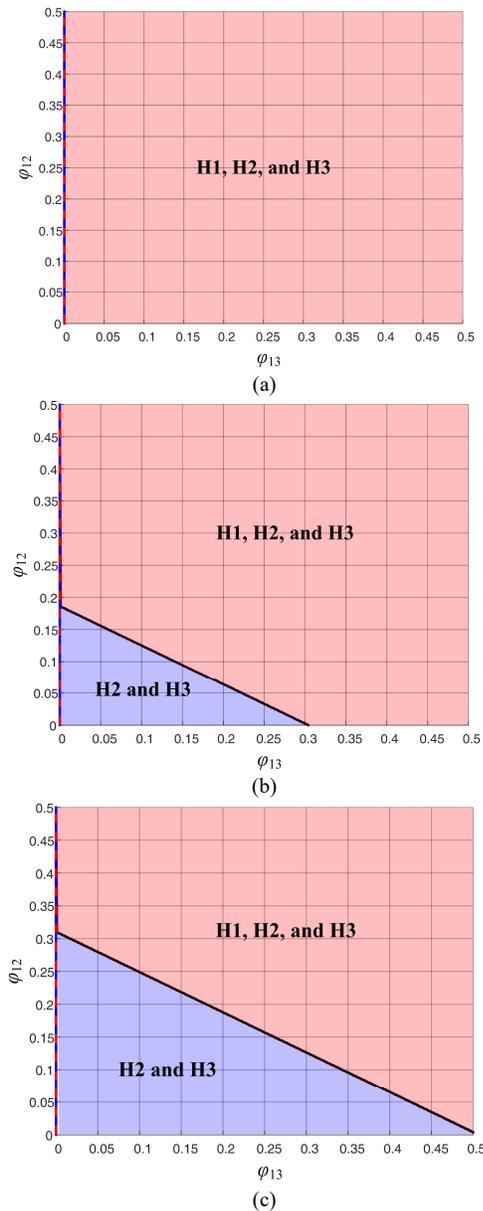


Fig. 3. ZVS region for the TAB converter: (a) $U_{in1}=1300$ V, (b) $U_{in1}=1000$ V, and (c) $U_{in1}=800$ V.

III. THE DESIGN OF THE H-BRIDGE PEBB

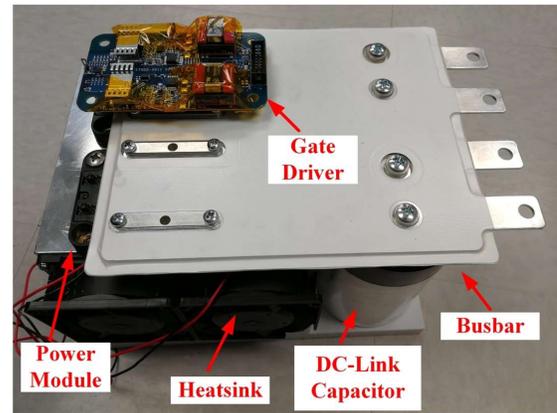
A. Turn-Off External Gate Resistance Design

Fig. 4(a) shows a picture of the H-bridge PEBB, which consists of two 1.7 kV SiC half-bridge modules, as shown in Fig. 4(b), two dc-link capacitors, and a heatsink. In this design, two 1500 V 195 μ F film capacitors DCP6S06195E000 from WIMA are adopted [21], as the film capacitors could provide better high-frequency performance compared with the conventional electrolytic capacitors. Meanwhile, compared with the ceramic capacitors, the film capacitor could achieve higher capacitance with lower volume and cost. The rated current of the dc-link capacitor is 40 A (RMS value). Based on the simulation, the maximum ripple current that flows through the dc-link capacitor is about 60 A when the output power is highest, which means that two dc-link capacitors could provide enough current rating. The selection of the capacitance should

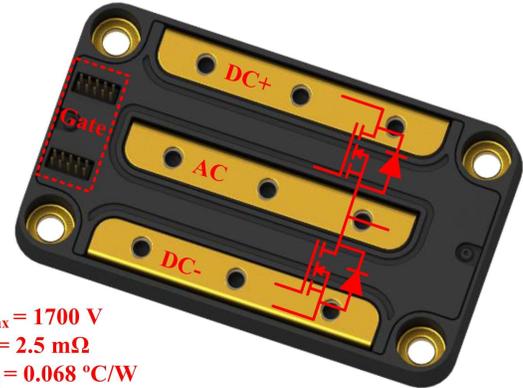
consider the voltage ripple on the output terminal. Ignoring the high-frequency harmonics of the output voltage and current, and only considering the fundamental voltage and current, which are in the switching frequency, i.e., 20 kHz, the voltage ripple on the output terminal could be approximated as [22]

$$\Delta V_{p-p} = \frac{P_{out}}{\omega V_{avg} C},$$

where ΔV_{p-p} is the peak-peak value of the output ripple voltage, P_{out} is the output power, V_{avg} is the average output voltage, ω is the switching frequency, and C is the dc-link capacitance. When the output power is 150 kW, switching frequency is 20 kHz, and the average output voltage is 1300 V, the output voltage ripple is about 2.4 V with the 390 μ F dc-link capacitor.



(a)



(b)

$V_{DSmax} = 1700$ V
 $R_{dson} = 2.5$ m Ω
 $R_{th,j-c} = 0.068$ $^{\circ}$ C/W

Fig. 4. (a) H-bridge PEBB, and (b) 1.7 kV SiC power module.

The power module used in this work is the 1.7 kV half-bridge module. The preliminary testing data can be found in [23]. The maximum continuous drain current is 680 A when the case temperature is 25 $^{\circ}$ C, while the on-state resistance of the module is 2.5 m Ω when the junction temperature is 25 $^{\circ}$ C. The input capacitance, output capacitance, and reverse transfer capacitance at 1000 V are 51 nF, 1.4 nF, and 12 pF, respectively.

The SiC module is driven by its companion gate driver CGD1700HB3P-HM3 [24], which can provide ± 14 A peak driving current. The stock value for the turn-on and turn-off gate resistances on the gate driver are $R_{g,on} = 5$ Ω and $R_{g,off} = 2.5$ Ω respectively. The busbar connecting the power modules and dc-link capacitors is designed to reduce the loop inductance and

attenuate the voltage overshoot during the turn-off transient and the stray inductance of the busbar is about 5 nH. Two isolated gate drivers are directly mounted on the top of the power modules.

It can be seen from Fig. 3 that the TAB converter can operate at the ZVS mode with the SPS scheme. However, it should be noted that the turn-off loss E_{off} still exists. Especially when the TAB converter utilizes a high switching frequency to improve the power density, the excessive turn-off loss will reduce the converter efficiency and lead to the junction temperature rise. The most common method to reduce the turn-off loss is decreasing the external gate resistance on the gate driver, which can increase the speed of the turn-off transient and reduce the switching loss [25]. Fig. 5 shows the switching energy of the power module under different turn-on gate resistance $R_{g,on}$ and turn-off gate resistance $R_{g,off}$. As mentioned earlier, the TAB converter could achieve the ZVS operation, while the turn-off energy loss still exists. Reducing $R_{g,off}$ from 2.5 Ω to 1 Ω can significantly decrease E_{off} , and thus, the converter efficiency can be improved. However, lower gate resistance will increase the voltage overshoot during the turn-off transient. Meanwhile, the lower gate resistance will also increase the peak driving current, which should be within the limit of the gate driver. Thus, detailed switching performance characterization should be conducted to determine the optimal gate resistance.

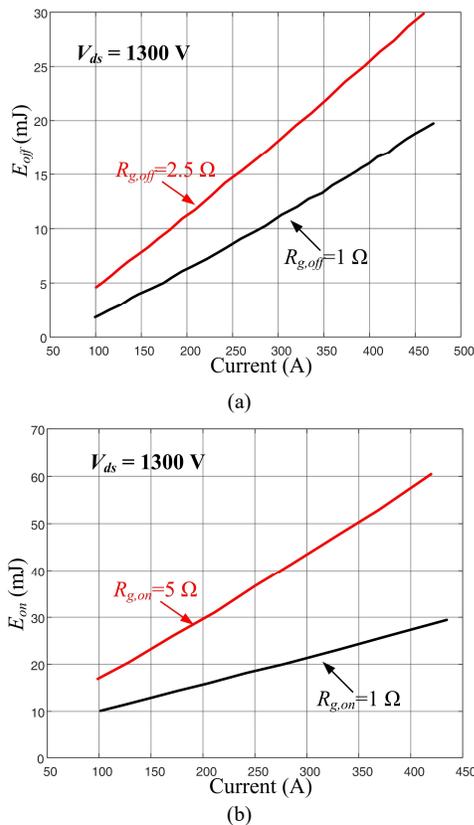


Fig. 5. Switching energy of the module under different gate resistance: (a) turn-off energy and (b) turn-on energy.

Fig. 6(a) illustrates the schematic of the clamped inductive load (CIL) test setup, where C_{gs} , C_{ds} , and C_{gd} are the junction capacitors of the module, L_{module} is the stray inductance of the

power module, L_{busbar} and R_{busbar} are the stray inductance and resistance of the busbar, respectively, and C is the dc-link capacitor, whose stray inductance and resistance are marked as L_C and R_C , respectively. Due to the loop stray inductances $L_{total} = L_C + L_{busbar} + L_{module}$ and device output capacitance $C_{oss} = C_{ds} + C_{gd}$, the commutation current during the turn-off transient will result in the LC circuit resonance, and voltage overshoot and oscillation will occur during the device turn-off transient [11]-[13]. Fig. 6(b) shows the CIL test result when $R_{g,off} = 1 \Omega$, and the dc-link voltage is set to be 1300 V. The module drain-source voltage V_{ds} is directly measured on the module terminals. It can be seen that the maximum voltage overshoot when the module is turned off at 535 A is about 1440 V, which is much lower than the maximum drain to source voltage, 1700 V. Besides, as mentioned earlier, the RMS value of the H-bridge output current is about 135 A when the TAB converter delivers full power, which is much lower than the test condition 535 A. Thus, the voltage overshoot caused by the lower $R_{g,off}$ is still acceptable. As the TAB converter can operate at the ZVS mode, the turn-on gate resistance is set as its stock value, i.e., $R_{g,on} = 5 \Omega$, to reduce the EMI caused by the dv/dt .

Fig. 7 shows the switching performance comparison under different $R_{g,off}$. It can be seen that the voltage overshoot during the turn-off transient with different $R_{g,off}$ have very limited differences due to the ultra-low stray inductance of the busbar, while the turn-off loss can be significantly reduced when $R_{g,off} = 1 \Omega$ is applied. Thus, the turn-off external gate resistance is selected as 1 Ω to reduce the switching loss while having acceptable voltage overshoot.

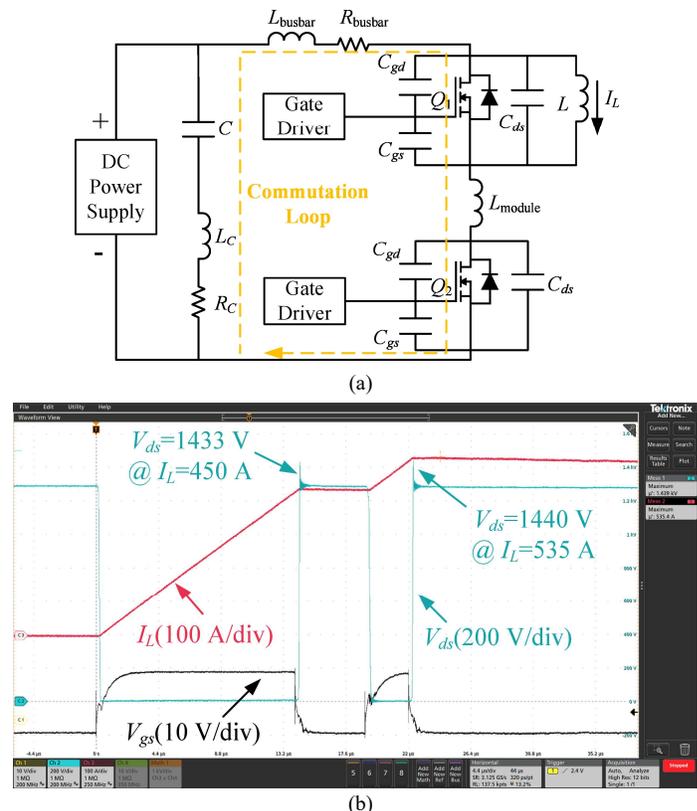


Fig. 6. (a) Schematic of the CIL test setup, and (b) Switching performance of the power module when $R_{g,off} = 1 \Omega$.

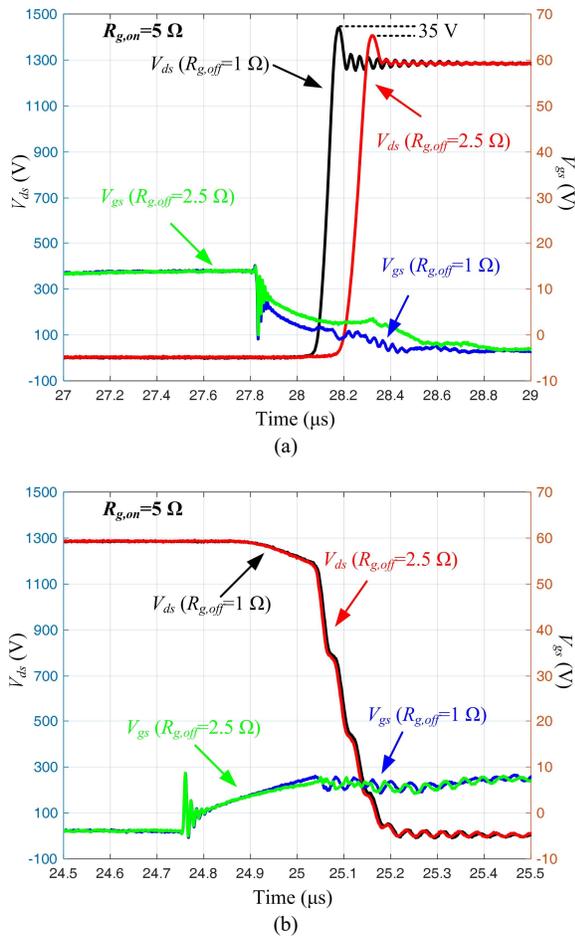


Fig. 7. Switching performance of the power module under different $R_{g,off}$: (a) turn-off transient and (b) turn-on transient.

B. Thermal Performance Characterization

To satisfy the high output power demand, the heatsink of the PEBB should provide a low resistance thermal path for the module power dissipation. Fig. 8 shows the equivalent thermal circuit of the PEBB, where T_j and T_c are the junction and case temperatures of the module, respectively, T_a is the ambient temperature, P_{loss} is the power loss of the module, $R_{th,j-c}$, $R_{th,TIM}$, and $R_{th,heatsink}$ are the thermal resistances of the power module, thermal interface materials (TIM), and heatsink, respectively. The junction temperature of the power module satisfies

$$T_j = T_a + (R_{th,TIM} + R_{th,heatsink})P_{loss} + \frac{1}{2}R_{th,j-c}P_{loss}, \quad (11)$$

supposing the power module has balanced power loss, i.e., the loss of the top switch is the same as that of the bottom switch, which is $P_{loss}/2$. It can be seen that under a certain ambient temperature, the junction temperature is determined by the module power loss and the total thermal resistance from the junction to the ambient. The thermal resistance of the power module $R_{th,j-c}$ can be found from the device datasheet. However, the thermal resistances of the TIM and heatsink vary with TIM thicknesses and air flow rates. Thus, the thermal characterization of the TIM and heatsink has been conducted to measure the thermal resistances. In this design, a heatsink with axial fan from Fischer Elektronik is adopted [30]. Fig. 9(a)

shows the setup of the thermal characterization test, where the power module is mounted on the heatsink with TIM applied. The TIM application procedure follows the manufacturer recommendation [31]. The module is forced turn-on and high load current can flow through the power module, which leads to a measurable power loss on the module. Thermocouples are used to measure the case temperature of the power module, and Fig. 9(b) shows the characterization result. The total thermal resistance from the module case to ambient $R_{th,c-a} = R_{th,TIM} + R_{th,heatsink}$ is about 0.12 K/W with the default 80 m³/h air flow rate, and the maximum power dissipation of the power module with 25 °C ambient temperature is about 975 W.

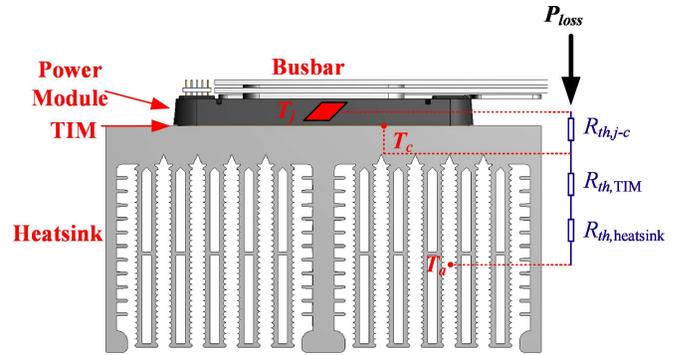


Fig. 8. Equivalent thermal circuit of the PEBB.

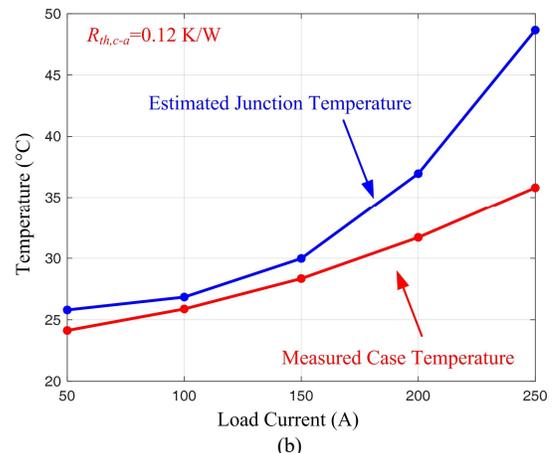
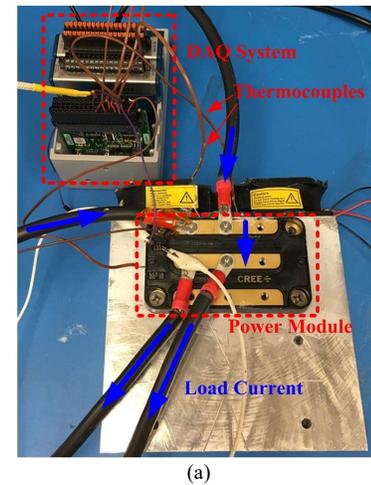


Fig. 9. (a) Thermal characterization test setup, and (b) Thermal performance of the TIM and heatsink.

IV. DESIGN OF THE HF THREE-PORT TRANSFORMER

A. Transformer Modeling and Design

In this design, nanocrystalline cores were used, which can provide high saturation flux density with low loss, and thus, both the high power density and high efficiency are achievable [1]. Fig. 10 shows the structure of the three-port transformer, where the core dimensions are represented by (A, B, F, G, D, E) , the secondary-side winding is placed between two primary-side windings, D_s and D_p are the conductor diameters of the secondary and primary windings, respectively. Given that the number of turns in both the primary- and secondary-side windings is N_p for the required turns ratio of 1:1:1. In order to optimize the transformer design, customized cores are used in this design, and dimensions of the core satisfy $E = D/2$, $F = D_p(3 + K_{ext})$, $A = F + D$, $G = D_p(N_p + K_{ext})$, and $B = G + 2E$, where $K_{ext}=1$ is the coefficient used to accommodate the needed extra space for the bobbin and insulation. In order to reduce the high-frequency skin effect loss, Litz wire is used for the windings. With the aim of keeping low copper loss and reducing the building complexity, the same type Litz wire is used for all windings. Considering the switching frequency is 20 kHz, the strand size of the Litz wire is set as 36 AWG, which is suitable when the operating frequency is between 20 kHz and 50 kHz [35], [36]. A commercially available Litz wire with $S = 4000$ strands is selected in this design, and the maximum wire current density is less than 3 A/mm² to reduce the conduction loss and temperature rise [27]. With the selected Litz wire, the conductor diameters are $D_s = D_p = 12.39$ mm considering the wire insulation. With core size definition and Litz wire specification, the design of the three-port transformer only relies on two parameters: number of turns N_p and core thickness D .

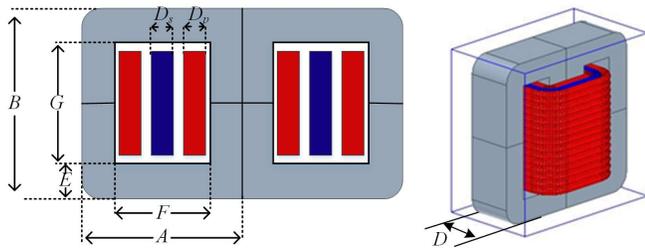


Fig. 10. Transformer structure.

As one of the core components of the TAB converter, the three-port transformer should achieve high efficiency and maintain a low volume to improve the power density. The loss of the transformer mainly consists of copper loss P_{cu} and core loss P_{fe} . The copper loss can be estimated as

$$P_{cu} = \frac{\rho_{cu} N_p}{A_{Litz}} \left[\frac{l_{p1} + l_{p2}}{S} I_p^2 + \frac{l_s}{S} I_s^2 \right], \quad (12)$$

where l_{p1} , l_{p2} , and l_s are the mean length per turn of the primary and secondary windings, respectively, I_p and I_s are the current of the primary and secondary windings, respectively, and $\rho_{cu}=1.68 \times 10^{-8}$ Ω/m is the resistivity of copper. Based on the geometric size of the core shown in Fig. 10, the mean lengths per turn satisfy $l_{p1}=4(D+D_p)$, $l_{p2}=4(D+3D_p)$, and $l_{p2}=4(D+5D_p)$. By using the Improved Generalized Steinmetz Equation (iGSE)

[17], the core loss can be estimated as

$$P_{fe} = k_i V_{fe} F_{sw}^\alpha B_{max}^\beta, \quad (13)$$

where

$$k_i = \frac{2^{\alpha+1} K_c}{\pi^{\alpha-1} \left(1.1044 + \frac{6.8244}{\alpha + 1.354} \right)}, \quad (14)$$

which is the numerical solution of

$$k_i = K_c \int_0^{2\pi} \left(2^{\alpha-1} \pi^{\alpha-1} \int_0^{2\pi} |\cos(\theta)|^\alpha 2^{\beta-\alpha} d\theta \right).$$

In (13) and (14), α , β , and K_c are the core Steinmetz coefficients, which are given in Table II, $V_{fe}=2D[D+D_p(N_p+5)]$ is the volume of the core, $F_{sw}=20$ kHz is the switching frequency, $B_{max}=V_{max}/(4F_{sw}N_pA_c)$ is the maximum flux density, and $A_c=D^2K_{eff}$ is the core effective cross-sectional area.

TABLE II. CORE PARAMETERS

Symbol	Value
α	1.2077
β	1.6456
K_c	2.2991
K_{eff}	0.78

According to the (12)-(14), the relationship between total transformer power loss P_T and transformer design parameters (D, N_p) can be written as follows

$$P_T(D, N_p) = P_{cu} + P_{fe}. \quad (15)$$

Besides the converter efficiency, the transformer loss P_T can also affect the temperature rise of the transformer. Considering that the heat generated by the transformer is dissipated through convection, the estimated temperature rise ΔT can be determined by

$$\Delta T = \frac{P_T}{hA_{surf}}, \quad (16)$$

where h is the empirical heat transfer coefficient, which is 22 W/(m²K) in this design, and A_{surf} is the surface area of the transformer [18]. Considering the total volume of core and winding and assuming A_{surf} corresponds to the surface area of a sphere, the surface area of the transformer can be expressed as

$$A_{surf} = \sqrt[3]{36\pi (V_{fe} + V_{winding})^2} \quad (17)$$

where volume of the winding $V_{winding} = 3\pi D_p^2 N_p (D + 3D_p)$.

Similar to the power loss, the transformer design parameters (D, N_p) determine the surface area, and thus, the temperature rise is also affected.

Fig. 11 (a)-(c) illustrates the relationship among transformer volume, power loss, temperature rise, core thickness, and number of turns. The transformer volume is calculated as

$$V_T = D^2 \left[2D + D_p (N_p + 9) \right] + D_p (N_p + 1) (D + 8D_p) (D + 6D_p) \quad (18)$$

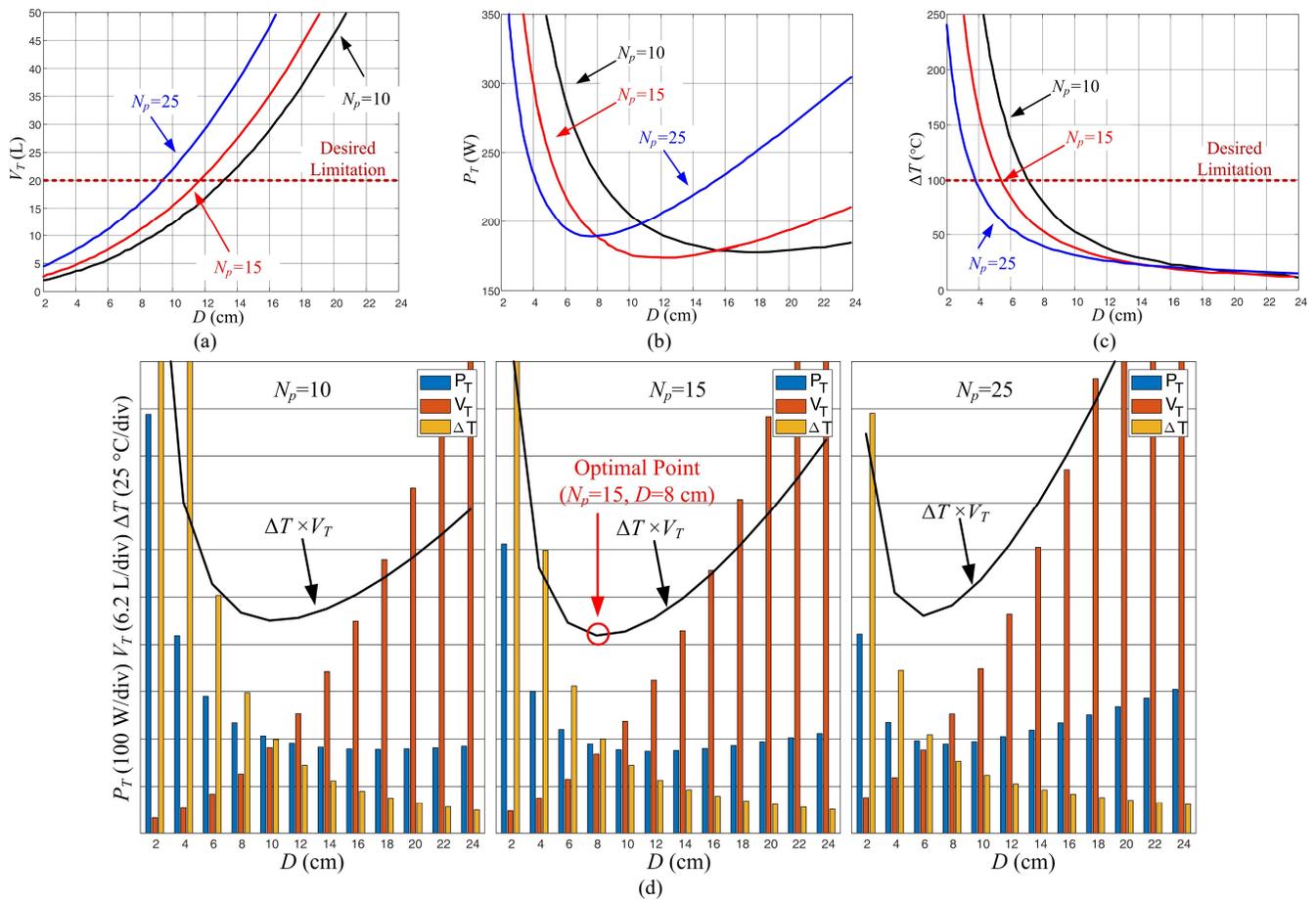


Fig. 11. (a) Transformer volume V_T , (b) Transformer power loss P_T , (c) Transformer temperature rise ΔT , and (d) co-optimization of the transformer with different core thickness D and number of turns N_p .

Compared with the total volume of the core and winding, the transformer volume V_T also considers the extra space for bobbin and insulation. In order to maintain relatively high power density and improve the system reliability, the desired transformer volume should be less than 20 L, and the temperature rise should not be more than 100 °C. However, it can be seen from Fig. 11(a) and (c) that the reduction of the transformer volume conflicts with the reduction of the transformer temperature rise, as a larger transformer volume would provide more surface area, which could reduce the transformer temperature rise based on (16). Thus, to address the tradeoff between the temperature rise and transformer power density, a volume-thermal co-optimization procedure has been conducted, and the result is given in Fig. 11(d). In Fig. 11(d), the product of transformer volume and temperature rise, i.e., $\Delta T \times V_T$ is used as the design cost function, as it can represent the tradeoff between transformer volume and temperature rise. It can be seen that the cost function can be minimized when $N_p=15$ and $D=8$ cm. Thus, in this work, the transformer design parameter is selected as $N_p=15$ and $D=8$ cm, which can maintain low power loss and temperature rise with a small total volume.

B. Transformer Characterization

To verify the effectiveness of the proposed design and characterize the transformer loss, both short-circuit (SC) and

open-circuit (OC) tests have been conducted. Fig. 12 depicts the 150-kW three-port transformer prototype and test setup.

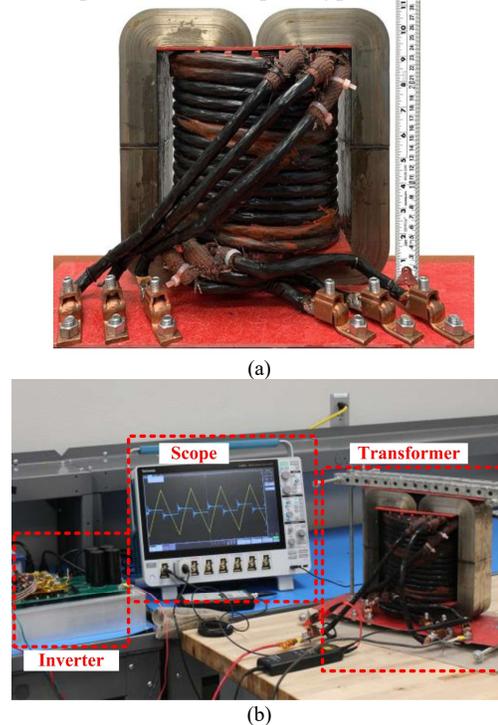
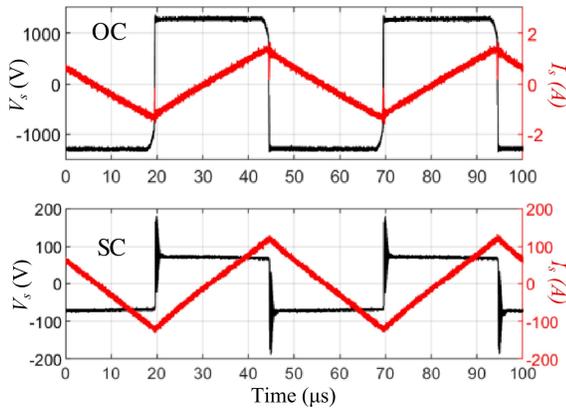
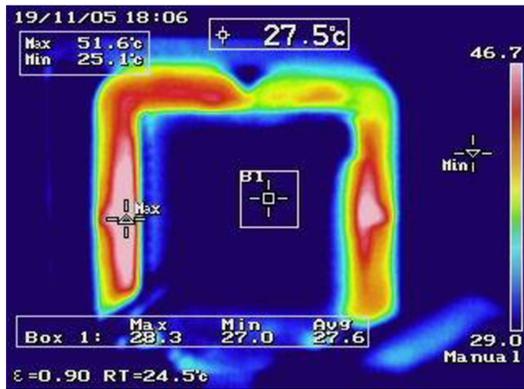


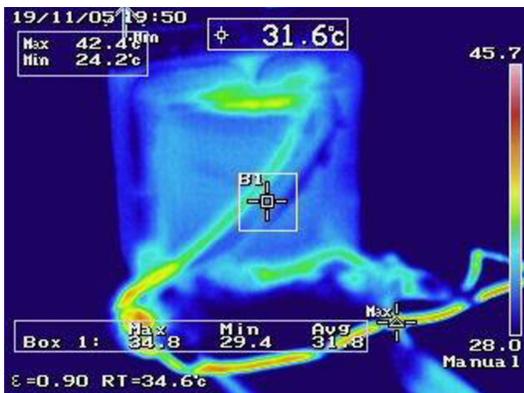
Fig. 12. (a) 150-kW three-port transformer prototype and (b) its test setup.



(a)



(b)



(c)

Fig. 13. (a) OC and SC tests waveforms, and thermal images of (b) OC test and (c) SC test.

An H-bridge converter applied 1300 V 50% duty-ratio 20 kHz square wave voltage to the transformer primary winding during the OC test, while the secondary side is open. In the SC test, the secondary winding is shorted, and a high SC current is generated by the H-bridge converter and flowing through the primary winding.

Fig. 13 shows the test results. The measured core loss during the OC test is $P_{oc}=129$ W, and the magnetizing inductance is $L_m=12.5$ mH. For the same condition, the estimated core loss given by (13) is $P_{fe}=118$ W, which is close to the measured result. In order to match with the actual application, the SC current RMS value is set as 67.5 A. The measured winding resistance is $R_{sc}=10$ m Ω , and the leakage inductance of the

transformer is about 3.5 μ H. Fig. 14 shows the design flowchart of the transformer. More details on transformer design and characterization can be referred to in [27].

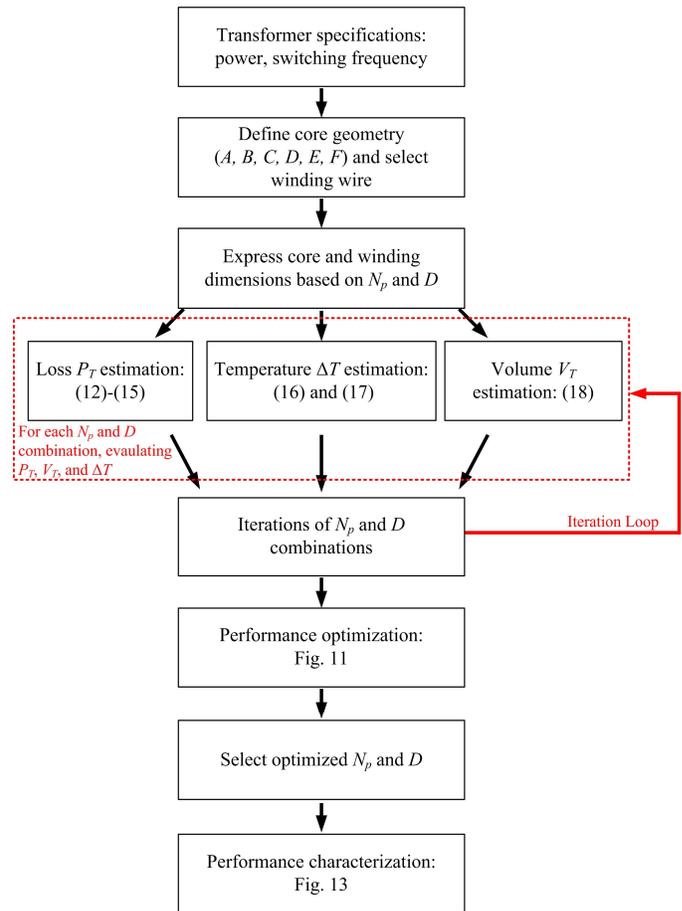


Fig. 14. Transformer design flowchart.

C. Design of External Inductors

According to the results of the transformer characterization, the leakage inductance of the transformer is 3.5 μ H per port. However, as mentioned earlier, the required inductances are $L_1=19$ μ H, $L_2=19$ μ H, and $L_3=31$ μ H, based on the converter power requirement. Thus, external inductors are adopted in this design to meet the inductances requirement. The required external inductances at those three ports are $L_{ind1}=15.5$ μ H, $L_{ind2}=15.5$ μ H, and $L_{ind3} = 27.5$ μ H, respectively. In order to avoid core saturation, an air gap is added to the inductor cores. With the air gap, the maximum flux density of the inductor can be expressed as [38]

$$B_{max} = \frac{NI_{max}\mu_0}{l_{gap}}, \quad (19)$$

where B_{max} is the maximum flux density, N is the number of turns, I_{max} is the peak current on the inductor, μ_0 is the vacuum permeability, and l_{gap} is the thickness of the air gap. The thickness of the air gap can be calculated by [38]

$$l_{gap} = \frac{\mu_0 A_c N^2}{L_{req}}, \quad (20)$$

where A_c is the core cross-sectional area and L_{req} is the required

inductance. Same as the transformer windings, the Litz wire with 4000 strands of 36 AWG is used as the inductor winding to reduce the high-frequency skin effect loss. Following the same core dimension definition shown in Fig. 10, the volume of the inductor core i.e., $V_{fe,ind}$ and winding, i.e., $V_{winding,ind}$ can be calculated as

$$\begin{cases} V_{fe,ind} = D(D + 3D_p)[D + D_p(N + 1)] \\ V_{winding,ind} = \pi D_p^2 N(4D_p + D) \end{cases}, \quad (21)$$

respectively. The copper loss of the inductor can be estimated as

$$P_{cu,ind} = \frac{\rho_{cu} N}{A_{Litz}} \left(\frac{4D_p + D}{S} I_{ind}^2 \right), \quad (22)$$

where I_{ind} is the inductor current, which satisfies $I_{ind}=I_p$ at the primary side and $I_{ind}=I_s$ at the secondary side. The core loss of the inductor can be estimated through iGSE as

$$P_{fe,ind} = k_{in} D^{1-2\beta} N^{-\beta} (D + 3D_p) [D + D_p(N + 1)], \quad (23)$$

where $k_{in} = 2^\beta k_{eff}^\beta L_{req}^\beta k_i f_{sw}^\alpha$. Thus, the inductor loss can be written as $P_{ind}=P_{cu,ind}+P_{fe,ind}$.

Similar to the transformer temperature estimation shown in (17), the temperature rise of the inductor can be estimated as

$$\Delta T_{ind} = \frac{P_{ind}}{hA_{surf,ind}}, \quad (24)$$

where $A_{surf,ind} = \sqrt[3]{36\pi(V_{fe,ind} + V_{winding,ind})^2}$ is the surface area corresponding to a sphere that has the same volume as the inductor.

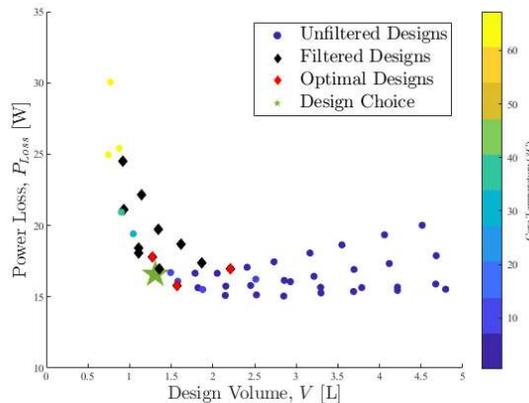


Fig. 15. Optimized design of the inductor.

Similar to the optimization procedure shown in Fig. 14, the optimization of the inductor is conducted and the results for the 15.5 μ H inductor is given in Fig. 15. The unfiltered data shown in Fig. 15 includes all the possible designs of the inductor under different D and N combinations, and a filter is adopted to limit the temperature rise to less than 80 $^{\circ}$ C and the thickness of the air gap less than 4 mm. Similar to the transformer design, a cost

function is defined as $V_{ind} \times \Delta T_{ind}$ is adopted to address the tradeoff between inductor volume and temperature rise, and the optimal D and N combinations are marked as red in Fig. 15. The output port inductor can be designed in the same approach. The core thickness D is 25 mm, and the thickness of the air gap is 1.8 mm. The number of turns for the 15.5 μ H inductor is 8, which is 10 for the 27.5 μ H inductor.

V. EXPERIMENTAL STUDIES

To evaluate the performance of the proposed TAB converter design, detailed experimental studies have been conducted. Fig. 16 shows the schematic and setup of the pump-back test, which utilize a dc power supply to clamp the dc-link voltage and compensate the system loss. As Fig. 15(a) shows, the first input port could deliver power to the output port, while the output port could feed the power back to the first input port through the pump-back configuration, i.e., a power $P_{circulating1}$ circulating inside of the TAB converter. Similarly, another power $P_{circulating2}$ could circulate between the second input port and output port. Using the pump-back configuration, every port can deliver high output power, while the power circulates among the three ports. The dc power supply only needs to provide the converter loss, and thus, the power requirement of the dc power supply can be significantly reduced.

The converter loss can be calculated by measuring the dc power supply output voltage and current, i.e., $P_{loss}=V_{dc} \times I_{dc}$, where P_{loss} is the TAB converter loss, V_{dc} is the dc power supply output voltage, and I_{dc} is the dc power supply output current. The definition of the TAB converter output power used in the efficiency measurement depends on the operation mode. When both the PV port and battery port provide power to the output port, the output power of the TAB converter can be written as $P_{out}=P_3$. In contrast, when the PV port delivers power to both the output port and battery port, i.e., $P_2 < 0 < P_3$, the output power of the TAB converter is defined as $P_{out}=|P_2|+P_3$, as the battery is also the system load when charging the battery. With the measured loss, the TAB converter efficiency could be calculated as $\eta = P_{out}/[P_{out} + P_{loss}] \times 100\%$. The port power could be calculated based on the H-bridge input voltage and current, which can be measured by voltage and current probes. For example, the output power P_3 could be calculated as

$$P_3 = \frac{1}{T_s} \int_0^{T_s} v_{dc3}(t) i_{dc3}(t) dt. \quad (25)$$

The H-bridge input voltages, i.e., v_{dc1} , v_{dc2} , and v_{dc3} , are measured using Tektronix THDP0200 and THDP0100 high voltage differential probes, and the input currents, i.e., i_{dc1} , i_{dc2} , and i_{dc3} , are measured by the Tektronix TCP404XL current probe. The model of the oscilloscope is Tektronix MSO 58. The dc power supply output voltage and current could be directly read from the power supply control panel, while a Tektronix A622 current probe is also used to measure the dc current. The dc-link voltage is set as 1300 V, i.e., $U_{in1}=U_{in2}=U_{out}=1300$ V ignoring the voltage drop on the cable, and all the converter parameters are the same as those given in Table I. The ambient temperature during the test is 25 $^{\circ}$ C. A TI TMS320F28379D dual-core DSP is used as the controller, which receives the

phase-shift command from the host computer and generates the gate signals accordingly. Then the gate signals are transferred to and amplified by the gate driver to drive the power modules.

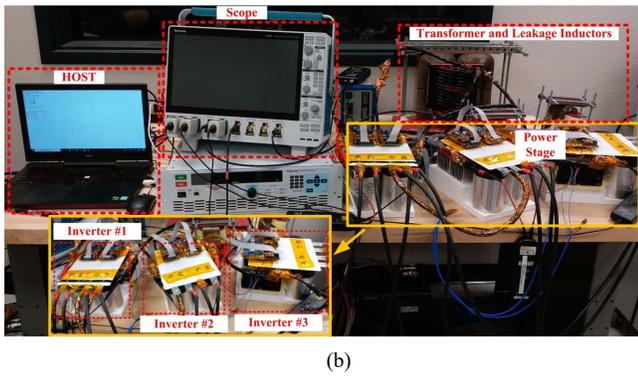
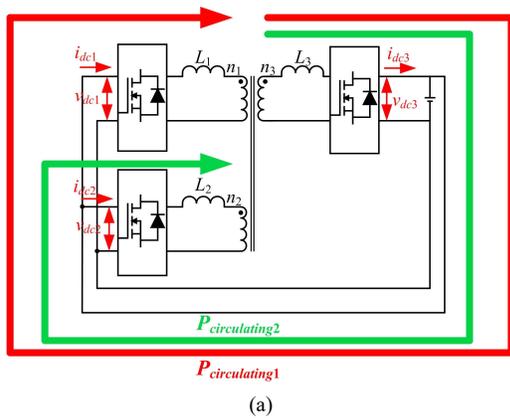


Fig. 16. The TAB pump-back test: (a) schematic and (b) test setup.

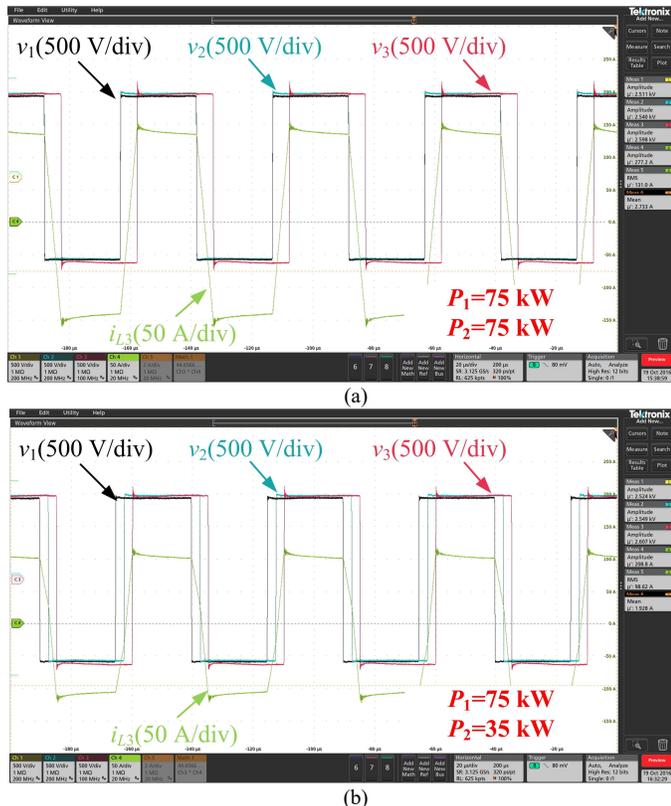


Fig. 17. Voltage and current waveforms of the TAB converter: (a) TAB converter outputs full power, and (b) The PV port outputs full power, and the battery port outputs 35 kW.

Fig. 17 shows the steady-state current and voltage waveforms of the TAB converter. It can be seen that the TAB converter can easily adjust the power distribution between two input ports to satisfy the power demand of the solar-plus-storage system by changing the phase-shift angles. Fig. 18 shows the device voltage V_{ds} and gate single V_{gs} of MOSFET Q_2 during the normal operation. It can be seen that the V_{ds} drops to zero before the rising edge of V_{gs} , thus the ZVS operation is achieved. Fig. 19 shows the transient response of the TAB converter. As mentioned earlier, the TAB converter could easily control the output power by adjusting the phase-shift angles between ports, and the result shows the TAB converter could increase the output power from 0 to full power within 2 ms.

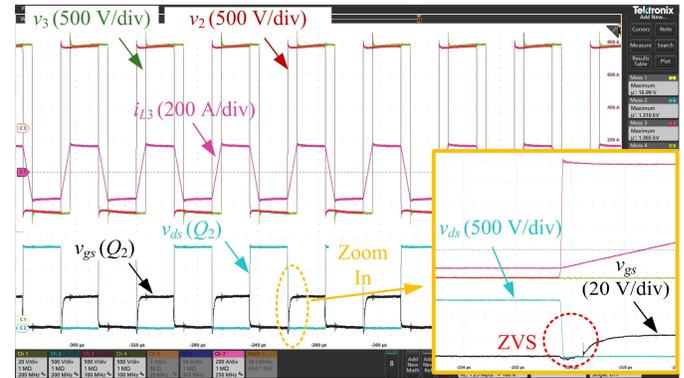


Fig. 18. ZVS operation of the TAB converter.

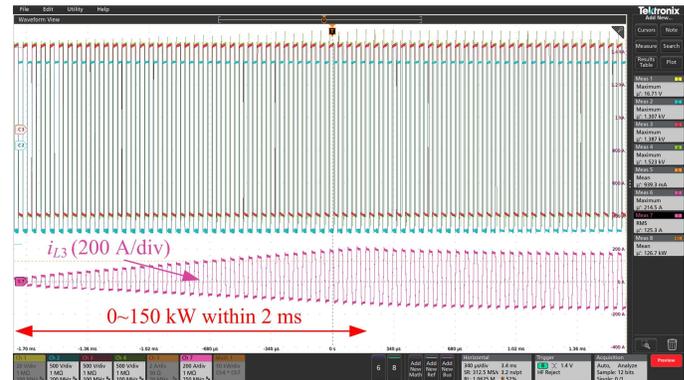


Fig. 19. Transient response of the TAB converter.

Fig. 20(a) shows the TAB converter efficiency with different $R_{g,off}$ when $P_1=P_2$, i.e., both input ports are used to deliver the same amount of power to the output port. As mentioned earlier, the lower $R_{g,off}$ could effectively reduce the switching loss and improve the system efficiency. In this mode, the TAB converter could achieve 99.1% peak efficiency at 50% load when $R_{g,off} = 1 \Omega$, and the full load efficiency is about 98.5%. Fig. 20 (b) presents the efficiency map of the TAB converter in different operation modes. Here the first input port is supposed as the PV input port. The second input port is the battery port, while the power P_2 can be positive or negative to represent the charging and discharging of the battery. It can be seen from the efficiency map that the proposed design could provide a wide 99% efficiency region.

Based on the test results when $R_{g,off} = 1 \Omega$, Fig. 21(a) shows the estimated power module junction temperature, and it can be

seen that all the power modules have more than 80 °C headroom to the device limitation. Thus, the reliability of the converter is verified. Fig. 21(b) shows the measured converter power loss with loss breakdown when $R_{g,off} = 1 \Omega$. The conduction loss of the TAB converter is calculated based on the on-state resistance of the power module, i.e., $P_{cond} = I^2 R_{dson}$, where I is the current that flows through the power module. The switching loss of the power module could be calculated as $P_{sw} = F_{sw} E_{off}(I)$, where the relationship between the current and turn-off energy could be found in Fig. 5.

As mentioned earlier, the transformer loss includes the core loss P_{fe} and copper loss P_{cu} . The core loss has been characterized through the OC test, which is about 129 W when the dc-link voltage is 1.3 kV and switching frequency is 20 kHz, and the copper loss could be calculated through $P_{cu} = I^2 R_{sc}$, where the winding resistance of the transformer R_{sc} also has been characterized through the SC test. The estimated external inductor loss is added into the transformer loss, as those external inductors are used to provide required leakage inductances. The cable loss is calculated through $P_{cable} = I^2 R_{cable}$, where R_{cable} is the measured resistance of the power cables. The high-power test of the TAB converter demonstrates the high efficiency of the proposed design, while all the power modules have relatively low temperature rise to ensure the system reliability.

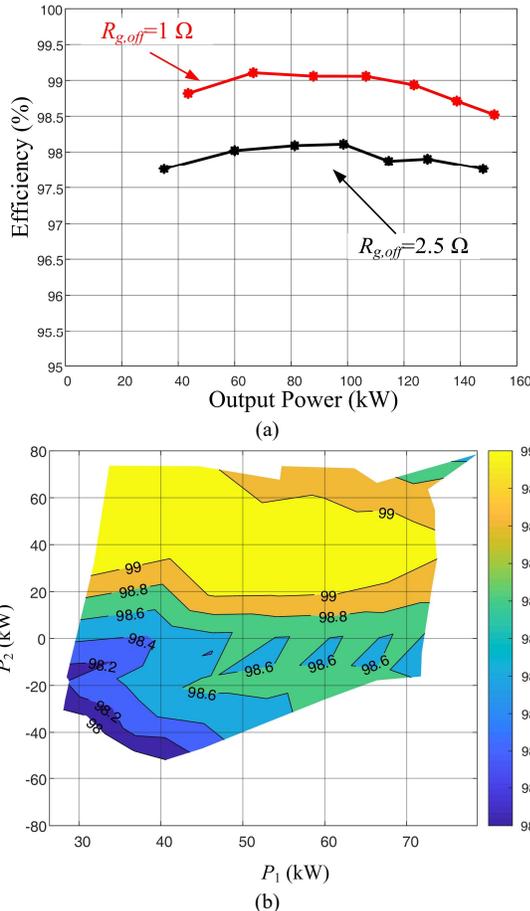


Fig. 20. TAB converter efficiency: (a) efficiency curve with different $R_{g,off}$ when $P_1=P_2$, and (b) efficiency map when $R_{g,off}=1 \Omega$.

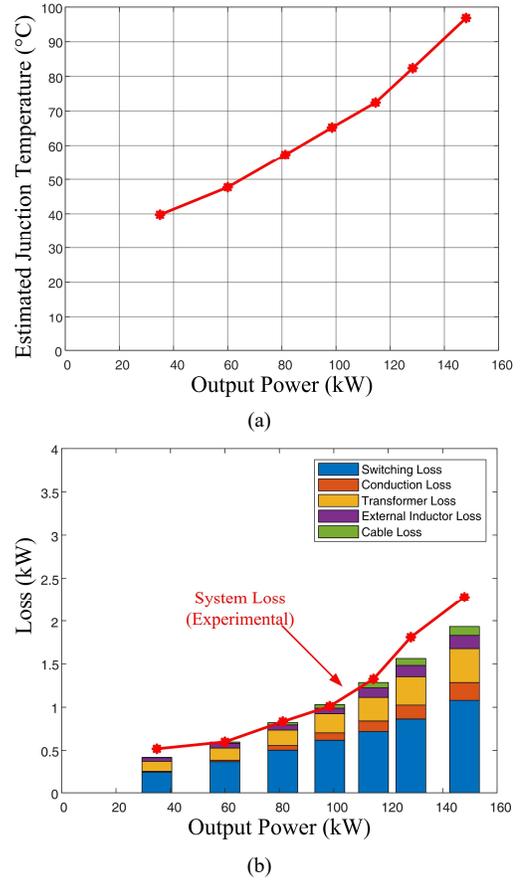


Fig. 21. (a) TAB converter estimated module junction temperature, and (b) TAB converter measured power loss and loss breakdown.

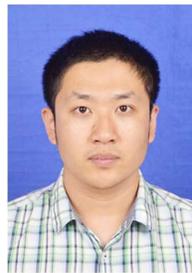
VI. CONCLUSION

To fulfill the high efficiency requirement of the solar-plus-storage systems, this paper presents detailed design, implementing, and testing of a SiC-based 150-kW 99% efficiency TAB converter. First, the review of the TAB converter has been presented, including the modulation scheme, power transmission characteristic, and soft-switching analysis. Then a SiC-based H-bridge converter PEBC has been designed and evaluated, which serves as the fundamental components of the TAB converter. Especially, evaluation and characterization on the gate resistance have been conducted to tradeoff between converter efficiency and transient voltage overshoot. In addition, the thermal performance of the PEBC also has been modeled and characterized to show the limit of power dissipation. Besides the PEBCs, the design of the three-port transformer, which couples PEBCs and deliver the power from input ports to the output port, has been given, as well as experimental characterization. Comprehensive experiment has been conducted on a fabricated TAB converter prototype to verify the proposed design, and 99.1% efficiency is achieved at 50% load, while the full load efficiency is 98.5%.

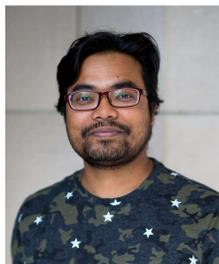
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